DATASHEET

RE31

13.56-MHz Multi-Standard RFID Reader IC

Rev 1.4

Features Summary

Highlight Features

Support Protocols

- ISO14443A/B, all bit rates
  - 106, 212, 424 and 848 kbps
- ISO15693, all modes
  - Downlink 1 of 4 and 1 of 256
  - Uplink 6.6/13/26/53 kbps with 1 & 2 sub-carrier
- NFC Tag Type 1 & PicoTag

Transmitter

- Proximity operating distance up to 10 cm (based on 3x4 cm^2 antenna)
- Modulation index adjustable by software
- Maximum driving current up to
  - 300 mA/ PIN @ 5V TVDD, 1 V drop
  - 400 mA/ PIN @ 7V TVDD, 1 V drop
- Accept external baseband signal for RF modulation
- Accept wide operating voltage for Tx from 2.7 - 7 V
- On-chip Framing coder

Receiver

- Rx sensitivity down to 1 mVpkpk
- Rx automatic gain control (AGC)
- EMD Suppress
- Enhancement BPSK decoder with Pattern Recognition
- RxMultiple
- ISO14443A/ISO15693 SOF searching
- On-chip Framing handler for supported standards

Interface and Peripheral

- SPI Interface up to 10 Mbps
- 64-byte send and receive FIFO-buffer
- 64-byte addressing user-configurable registers
- 256-byte EEPROM
- Interrupt (IRQ) PIN
- Programmable timer
- Programmable clock divider for external MCU
- Low jitter on-chip oscillator buffer
- On-Chip Dual 80 mA 3.3V Regulators

Operating Conditions

- Operating temperature from -40 to 85°C
- Operating voltage from 2.7 to 3.3 V for Receiver
- Operating voltage from 2.7 to 7 V for Transmitter
- 6.0 uA in power down mode
- 1.3 mA in standby mode
- 8.0 mA when all receiver blocks are active
- Small QFN5x5 32-Pin with Heat sink pad or TSSOP-28

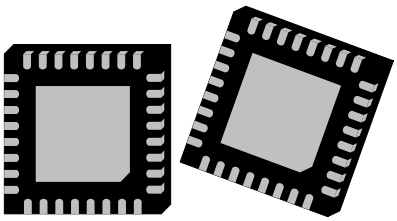
Reference Design/ Evaluation kit

- Ready- to-use USB Module and Generic module
- Demonstration Software/ Sample firmware available

Applications

- Contactless payment system
- Secure access control
- PC peripheral device
- Handheld RFID reader/Mid Range RFID reader

General Description



32-Pin QFN5x5 Package

The RE31 HiRead-R is a single-chip long-range reader ASIC for all popular 13.56-MHz RFID/contactless standard protocols. The HiRead-R supports and compatibles with all major global secured baseband ISO standards including ISO14443 Type A, Type B, Crypto_M, and Smartlabel ISO15693. The HiRead-R provides a hi-speed SPI controller/host interface with a built-in 64-byte FIFO for smooth data transfer. Furthermore, the embedded codec is capable of handling all bit-level coding/encoding, encrypting/decrypting as well as frame-level manipulation for transmission and reception. The chip is well suited for mobile devices due to its low power consumption and low operating voltage from 2.7-3.3 V. The dual on-chip 3.3V regulators are provided to stabilize the chip's power, and simultaneously supply the power to the external companion microcontroller up to 80 mA.

The HiRead-R receiver circuit incorporates a full AGC loop allowing a wide dynamic range of RF input signal levels. The chip's excellent sensitivity performance enables detection of the input signals with amplitudes as low as 1mVpkpk without distorting the data integrity. The receiver filters can be selected optionally either to a predefined band in accordance with the generic required standard setup, or to an arbitrarily defined combination which gives flexibility to cope with various antenna variations/parameters. The baseband circuits permit the inbound/outbound configuration to accept various forms of customized protocols, incoming to the chip and outgoing to the external RF circuitry in the application specific-design system. The HiRead-R transmitter is capable of accepting a wide range of operating supply voltages to serve various applications, e.g., 5V for base stations or desktop readers, and 3.3V for handheld devices. The transmission controller is entirely used to support all operation status and requests, including FIFO status full/high/low and Transmission/Reception complete. The transmitter drivers support a wide range of power supply voltages from 2.7 to 7 V. A high drive current up to 300 mA is guaranteed for demanding item-level mid-range reader designs. The dual high-powered transmitters can be flexibly configured in various configurations, e.g. differential driving, single-ended driving, and a mode to drive an external Class-E amplifier for improving the drive strength in the gate antenna setup.

To facilitate operation of the companion microcontroller, the HiRead-R is fully equipped with on-chip peripheral support devices such as an RF-trig timer; a host interrupt generator, and a clock divider. The chip's embedded 256-byte EPPROM stores predefined re-loadable register values for easy reader setup, and the crypto key for encryption mode. The RE31 is offered in a low-profile QFN package with excellent heat dissipation when self-mounted on PCB.

Revision History

Revision	Date	Description	Change/Updated/Comment
1.0	11 July 2017	1st Release	Official release
1.1	16 Aug 2018	Correction Error	Correct Cross Reference Error in 6.3.8 and 7.4.3
1.2	12 Feb 2019	Correction Error	Correct subcarrier signal strength (RSSI) level in 5.2.7 Change detail in Table 8-2 - test signal
1.3	05 Apr 2019	Update Electrical Spec	Add more detail for Table 3-3, Table 3-4, Table 3-5, Table 3-6, and Table 3-9 Update Analog Characteristic Figure 3-7
1.4	30 Dec 2021	Update ordering information	Change product part no. in 'Ordering Information' table

Ordering Information

Part No.	Description	Package	Marking	Part No.
PI5AVQO7P20UT3101E1	RE31-01, 13.56MHz RFID Reader IC Front-End ISO14443A/ISO14443B/ISO15693/NFCtag type 1/2/4/5 (2nd Gen.) QFN 0.85 mm, TnR, IC	32-PIN QFN 5x5 mm	**8JAYM**	Active
PI5ATSM6T10UT3101Y1	RE31-01, 13.56MHz RFID Reader IC Front-End ISO14443A/ISO14443B/ISO15693/NFCtag type 1/2/4/5 (2nd Gen.) TSSOP, Tube, IC	28-PIN TSSOP	**6GAYM**	Active

Content

List of Figures

List of Tables

0. Notation

0.1 Styles and Fonts for key words

This part defines styles and fonts used for the key words throughout this document. The key words are names of signal, register, pin, state of operation and command. The styles, fonts, and their indications are shown in Table 0-1.

Table 0-1: Style and Fonts key word

Symbol	Indication
Signal	Signal name
Register	Register name or Bit name
pin RX	Pin name
"State of Operation"	State of operation
Command	Command name in register 0x01

- To refer to a register address and a value in a register, a hexadecimal number proceeding with letter "0x" is used, for example 0x0A.
- To refer to a bit located in a register address, a symbol "." following by a number reflecting the bit location starting from 0 to 7 is used. For example, 0x0A.0 refers to bit 0, least significant bit, in the register 0x0A.
- To refer to a set of consecutive bits located in a register address, a format ".[msb:lsb]" is used after a register value. For example, a value of 0x0A.[3:0] refers to bit 3 ,2, 1, and 0 in the register 0x0A.
- To refer to a binary value in some registers, the letter "b" is placed at the end of the binary number, for example "1010b".

0.2 Abbreviation

Table 0-2: Abbreviation

Abbreviation	Term
AGC	Automatic gain control
CRC	Cyclic redundancy check
DPLL	Digital Phase locked Loop
EEPROM	Electrically Erasable Programmable Read-Only Memory
EGT	Extra guard time in ISO14443B
EOF	End of Frame
ETU	Elementary Time Unit
fc	Carrier frequency
FIFO	First In, First Out Memory
SOF	Start of Frame
UID	Unique Identifier

1. Functional Overview

The RE31 contains a transmitter, a receiver, a baseband processor, and a voltage regulator. The architecture of the RE31 is shown in Figure 1-1.

The transmitter contains integrated dual drivers, supporting operating voltages from 2.7 Volt to 7 Volt. The transmitter can be configured to support various antenna topologies such as differential driving, single-ended driving, and pre-driving for external class-E amplifiers. An on-chip coder can generate a variety of line-coding, namely Miller to support ISO14443A, NRZ to support ISO14443B, and 1-of-4 and 1-of-256 to support ISO15693. Moreover, a direct modulation from pin **SIGIN[0]** is allowed.

The receiver part consists of an on-chip envelope detector, a voltage reference generator, an on-chip oscillator, an amplifier-filter system, a filter tuning system, a BPSK-bit decoder, a Manchester-and-FSK decoder, a frame decoder, and a timing control generator. A receiver input, pin **RX**, can accept a carrier modulated signal or an envelope-demodulated signal from an external envelope detector. Employing an external envelope detector can yield an extended read range. With this flexibility, it enables a wide variety of RF connection topologies. The envelope of the input signal is filtered and amplified with optional control by an automatic gain control (AGC), resulting in an amplitude control to prevent shape distortion. The BPSK-bit decoder and Manchester-and-FSK decoder translates the amplified signal to the digital data. The bit data is then checked the validity and assembled into bytes by the digital frame decoder. Next, the complete and valid bytes are transferred into the FIFO. In case of the encryption, the Crypto_M engine is provided to encrypt and decrypt as well as execute the authentication process for the Crypto_M card.

The digital part contains an FIFO controller, a CRC generator, a programmable timer, an EEPROM, a state machine, and configurable registers in order to facilitate RF transmission and reception activities. The RE31 can be controlled and accessed through a 4-wire SPI interface and a register page with the communication speed up to 10 Mbps. An interrupt system and a pin **IRQ** are provided to support interrupt-oriented programming after the end of RF-activities.

In addition, there are two regulators for supplying analog and digital parts with 80 mA driving capability. A configurable clock output, of which the frequency can be 13.56, 6.78 or 3.39 MHz, is available via pin **CLKBF**.

1.1 Detail Block Diagram

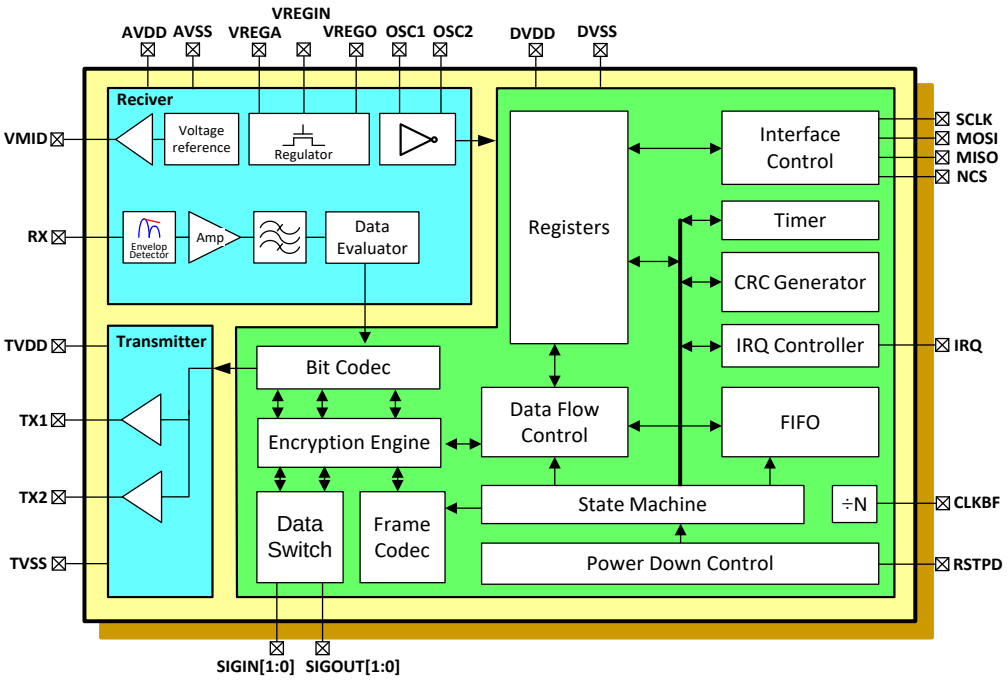


Figure 1-1: Functional block diagram

1.2 Typical Operating Circuit

A basic operating circuit and a typical usage of a close coupling application is illustrated in Figure 1-2. A differential antenna is directly connected from a RE31's transmitter driver, whereas the receiver senses the tag-modulated signal from envelope of RF carrier through the voltage divider. The RE31 is controlled by a microcontroller via an SPI interface. In addition, other circuit configurations such as class-E amplifiers with external envelope detectors or single-ended drivers can be implemented and will be described in section 8.1.

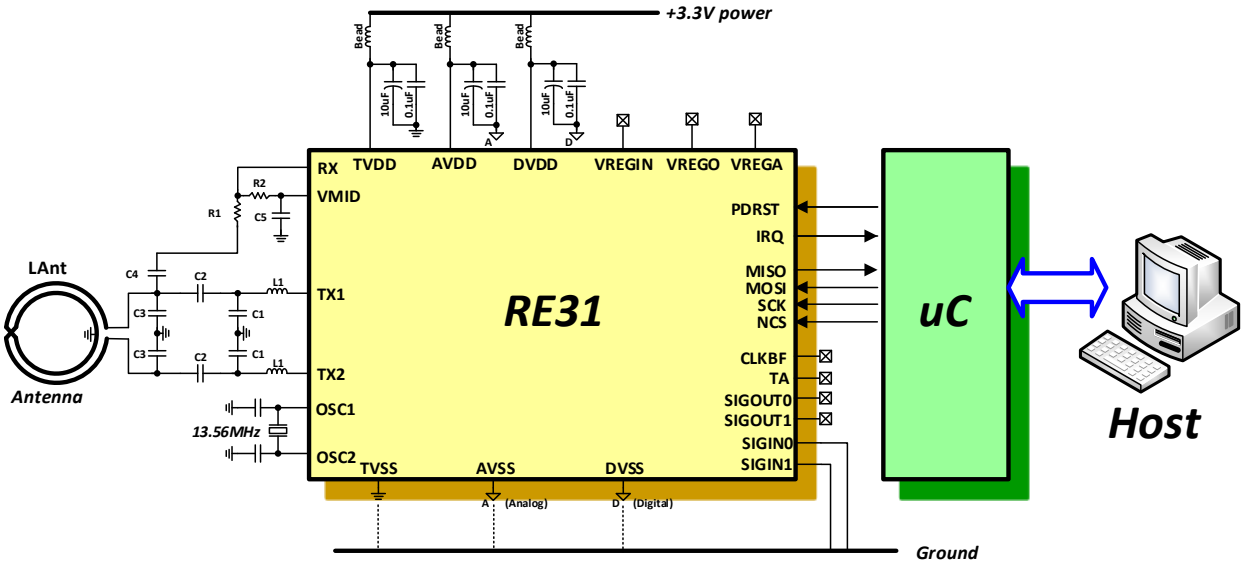


Figure 1-2: Typical operating circuit

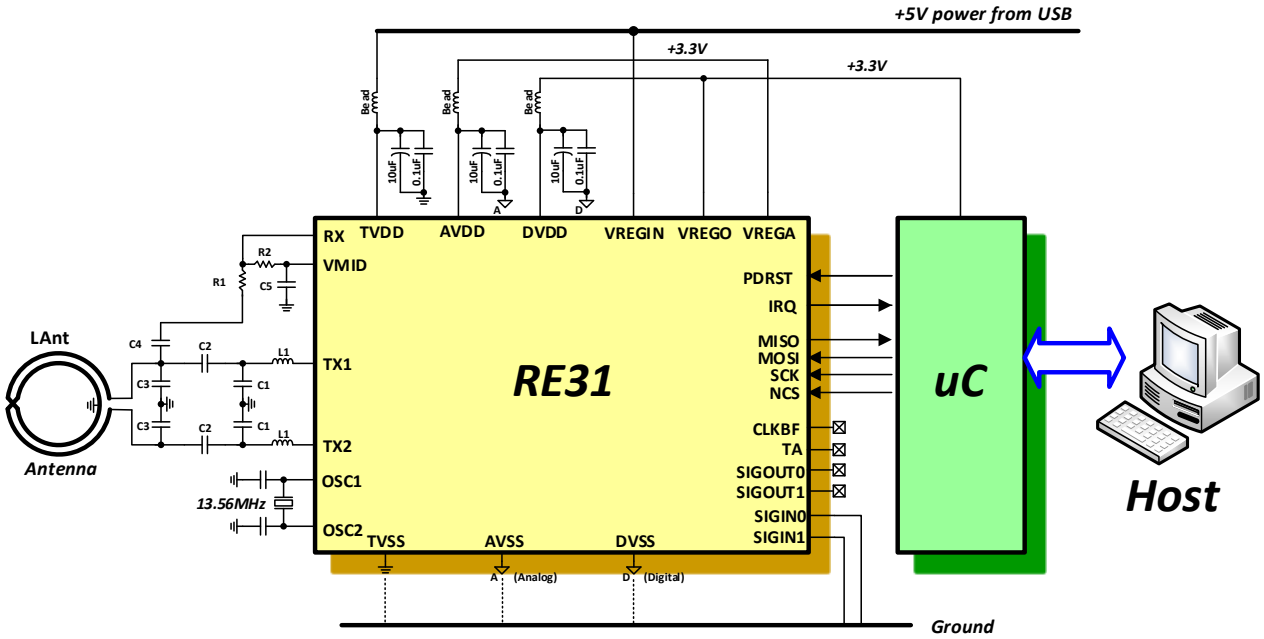


Figure 1-3: Typical configuration employing on-chip regulator

2. Pin Configuration

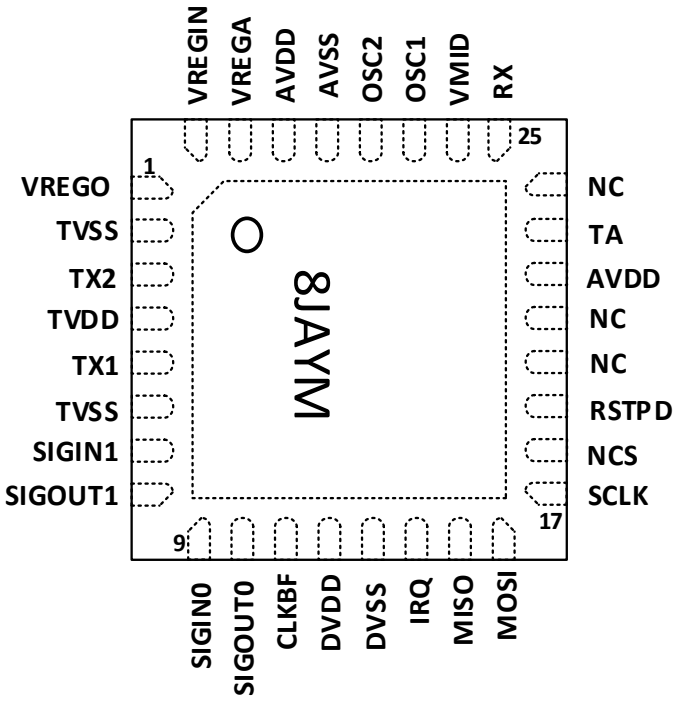


Figure 2-1: Pin arrangement (Top View)

A: Revision Code
Y : Year Code
M : Month Code

Table 2-1: Pin Description

Pin	Symbol	Type	Related SUPPLY	Description
1	VREGO	Power	DVDD, DVSS	3.3V Regulator Output for Digital part
2	TVSS	Power	TVDD, TVSS	Transmitter Ground
3	TX2	OUT	TVDD, TVSS	Transmitter Output 2
4	TVDD	Power	TVDD, TVSS	Transmitter VDD
5	TX1	OUT	TVDD, TVSS	Transmitter Output 1
6	TVSS	Power	TVDD, TVSS	Transmitter Ground
7	SIGIN1	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
8	SIGOUT1	OUT	DVDD, DVSS	Digital output signal for test mode
9	SININ0	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
10	SINOUT0	OUT	DVDD, DVSS	Digital output signal for test mode
11	CLKBF	OUT	DVDD, DVSS	Buffered clock 13.56/6.78/3.39 MHz Output for external MCU
12	DVDD	Power	DVDD, DVSS	Digital and I/O VDD
13	DVSS	Power	DVDD, DVSS	Digital and I/O Ground
14	IRQ	OUT	DVDD, DVSS	Interrupt Request
15	MISO	OUT	DVDD, DVSS	SPI Master-In-Slave-Out
16	MOSI	IN	DVDD, DVSS	SPI Master-Out-Slave-In
17	SCLK	IN	DVDD, DVSS	SPI Clock Input
18	NCS	IN	DVDD, DVSS	SPI Chip Select (Active low)
19	RSTPD	IN	DVDD, DVSS	Reset and Power Down (Active High)
20	NC	-	-	Not Connected
21	NC	-	-	Not Connected
22	AVDD	PWR	AVDD, AVSS	Analog VDD (Optional)
23	TA	OUT	AVDD, AVSS	Analog Test Pin
24	NC	-	-	Not Connected
25	RX	IN	AVDD, AVSS	Receiver Input
26	VMID	IN	AVDD, AVSS	Mid Rail Reference Voltage
27	OSC1	IN	AVDD, AVSS	Xtal Oscillator input
28	OSC2	OUT	AVDD, AVSS	Xtal Oscillator Output
29	AVSS	Power	AVDD, AVSS	Analog Ground
30	AVDD	Power	AVDD, AVSS	Analog VDD
31	VREGA	Power	AVSS	3.3V Regulator Output for Analog part
32	VREGIN	Power	AVDD, AVSS	Regulator input

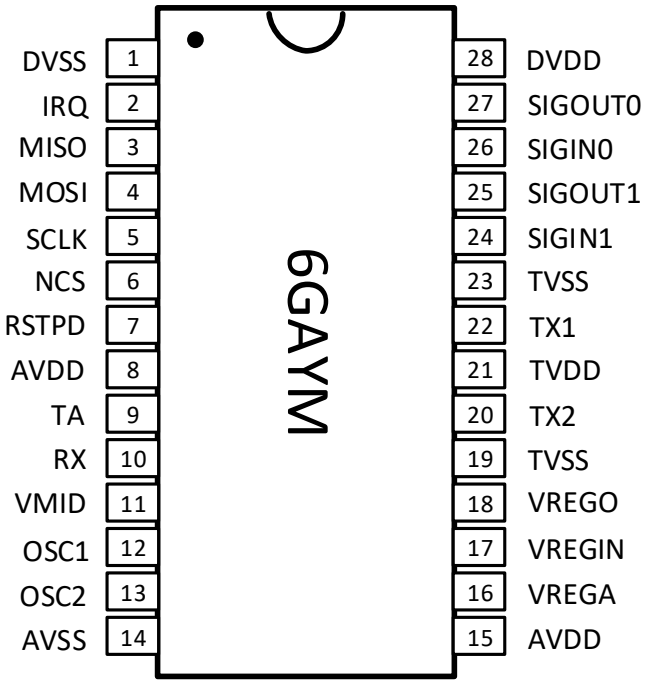


Figure 2-2: TSSOP Pin arrangement (Top View)

A: Revision Code
Y : Year Code
M : Month Code

Table 2-2: TSSOP Pin Description

Pin	Symbol	Type	Related SUPPLY	Description
1	DVSS	Power	DVDD, DVSS	Digital and I/O Ground
2	IRQ	OUT	DVDD, DVSS	Interrupt Request
3	MISO	OUT	DVDD, DVSS	SPI Master-In-Slave-Out
4	MOSI	IN	DVDD, DVSS	SPI Master-Out-Slave-In
5	SCLK	IN	DVDD, DVSS	SPI Clock Input
6	NCS	IN	DVDD, DVSS	SPI Chip Select (Active low)
7	RSTPD	IN	DVDD, DVSS	Reset and Power Down (Active High)
8	AVDD	PWR	AVDD, AVSS	Analog VDD (Optional)
9	TA	OUT	AVDD, AVSS	Analog Test Pin
10	RX	IN	AVDD, AVSS	Receiver Input
11	VMID	IN	AVDD, AVSS	Mid Rail Reference Voltage
12	OSC1	IN	AVDD, AVSS	Xtal Oscillator input
13	OSC2	OUT	AVDD, AVSS	Xtal Oscillator Output
14	AVSS	Power	AVDD, AVSS	Analog Ground
15	AVDD	Power	AVDD, AVSS	Analog VDD
16	VREGA	Power	AVSS	3.3V Regulator Output for Analog part
17	VREGIN	Power	AVDD, AVSS	Regulator input
18	VREGO	Power	DVDD, DVSS	3.3V Regulator Output for Digital part
19	TVSS	Power	TVDD, TVSS	Transmitter Ground
20	TX2	OUT	TVDD, TVSS	Transmitter Output 2
21	TVDD	Power	TVDD, TVSS	Transmitter VDD
22	TX1	OUT	TVDD, TVSS	Transmitter Output 1
23	TVSS	Power	TVDD, TVSS	Transmitter Ground
24	SIGIN1	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
25	SIGOUT1	OUT	DVDD, DVSS	Digital output signal for test mode
26	SIGIN0	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
27	SIGOUT0	OUT	DVDD, DVSS	Digital output signal for test mode
28	DVDD	Power	DVDD, DVSS	Digital and I/O VDD

3. Specifications

3.1 Absolute maximum rating

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for an extended period of time may affect the device reliability. Only one absolute maximum rating can be applied at a time.

Table 3-1: Absolute maximum rating

Parameter	Rating
Analog supply voltage (AVDD to AVSS)	-0.3 V to 3.6 V
Digital supply voltage (DVDD to DVSS)	-0.3 V to 3.6 V
Transmitter supply voltage (DVDD to DVSS)	-0.3 V to 3.6 V
Analog input voltage	-0.3 V to AVDD+0.3 V
Analog output voltage	-0.3 V to AVDD+0.3 V
Digital input voltage	-0.3 V to DVDD+0.3 V
Digital output voltage	-0.3 V to DVDD+0.3 V
Transmitter Output voltage	-0.3 V to TVDD+0.3 V
Operating Temperature Range	-40 °C to +85 °C
Storage Temperature Range	-65 °C to +150 °C
Junction Temperature	125 °C
Thermal Impedance (θ_{JA})(1) – QFN 5x5	36 °C/W
Thermal Impedance (θ_{JA})(1) – TSSOP-28	TDB

Note: θ_{JA} is determined by 2s2p 76.2x114.3-mm PCB following JEDEC51-5, -7

3.2 Electrical characteristic

Table 3-2: Operating condition

Parameter	Description	Min	Typ	Max	Unit	Conditions
AVDD	Analog Power Supply Voltage	2.7	3.3	3.6	V	
DVDD	Digital Power Supply Voltage	2.7	3.3	3.6	V	
TVDD	Transmitter Power Supply Voltage	2.7	5	7	V	
ESD	Electrostatic discharge tolerance	2			kV	HBM model
VPOR	Reset Trigger voltage		2.4		V	

Table 3-3: Power consumption

Parameter	Description	Min	Typ	Max	Unit	Conditions
			5.5		mA	All blocks active
			1.4		mA	Idle (Receiver Off)
			1.3		mA	Standby
			6.0	11.0	uA	Soft Power down
IAVDD	Analog Power Supply Current		0.5	1.0	uA	Hard Power down, (**RSTPD** = 1)
			2.5		mA	**CLKBF** is not enabled
			3.0		mA	**CLKBF** is enabled
			64		uA	Standby
IDVDD	Digital Power Supply Current		0.5	1	uA	Soft/Hard Power down

Table 3-4: Pin Characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
CRx	Rx input capacitance		10		pF	
IRx	Rx input Leakage current			1	uA	
Cindig	Digital Input Capacitance		10		pF	
VINL	Digital logic input Low voltage			0.8	V	DVDD = 3.3 V
VINH	Digital logic input High voltage	2.4			V	DVDD = 3.3 V
			0.04		V	DVDD = 3.3 V, ILoad (1) = 1 mA
VOL	Digital logic Output Low voltage		0.4		V	DVDD = 3.3 V, ILoad (1) = 10 mA
			3.26		V	DVDD = 3.3 V, ILoad (1) = 1 mA
VOH	Digital logic Output High voltage		2.86		V	DVDD = 3.3 V, ILoad (1) = 10 mA
Tr	Rise time		3	6	nS	DVDD = 3.3 V, CLoad(2) = 10 pF
Tf	Fall time		3	6	nS	DVDD = 3.3 V, CLoad(2)= 10 pF
Iinlogic1	Logic 1 input current			1	uA	VINH = DVDD
Iinlogic0	Logic 0 input current			1	uA	VINL = 0
Ioutlogic1	Logic 1 Output Source Current			15	mA	DVDD = 3.3 V
Ioutlogic0	Logic 0 Output Sink Current			15	mA	DVDD = 3.3 V

(1) ILoad : Load current at digital output pin

(2) CLoad : Load capacitance at digital output pin

Table 3-5: Transmitter

Parameter	Description	Min	Typ	Max	Unit	Conditions
		300	340		mA	TVDD = 5V, 85 °C
ITX1	Logic 1 Transmitter Source Current	380	440		mA	TVDD = 7V, 85 °C
		270	300		mA	TVDD = 5V, 85 °C
ITX0	Logic 0 Transmitter Sink Current	360	400		mA	TVDD = 7V, 85 °C
			3.5	5	Ohm	TVDD = 5V, 85 °C
ZTX	Tx Output impedance (**GsCfgCW** =0x3F)		2.5	4	Ohm	TVDD = 7V, 85 °C
ITVDD	Transmitter Static Power supply Current		7		mA	**TX1** & **TX2** are Unconnected **RF1En** = 1, **RF2En** = 1 TVDD = 5 V
			-	60	%	TVDD = 5V, **100ASK** = 0
M	Adjustable Modulation index			100	%	TVDD = 5V, **100ASK** = 1

Table 3-6: Receiver

Parameter	Description	Min	Typ	Max	Unit	Conditions
VSEN	Receiver input sensitivity		1		mVpkpk	AVDD = 3.3V
PSRR	Power supply rejection ratio		40		dB	AVDD = 3.3V + 0.2*sin(1MHz)
VRx	Rx input voltage range	0.0		3.3	V	AVDD = 3.3 Volt, **BypassENV** = 0
		0.5		2.8	V	AVDD = 3.3 Volt, **BypassENV** = 1
VCarMin	Minimum Carrier for envelope detector		0.3		Vpkpk	
VVMID	VMID Voltage		1.65		V	**VMidsel** = 0, AVDD = 3.3 V
			1.24		V	**VMidsel** = 1, AVDD = 3.3 V
ZVMID	VMID output impedance @ 13.56 MHz		6		ohm	CLoad(1) = 100nF, TVDD = 5 V
Gain	Gain (Measured from Rx to the output of the internal last amplifier)			48	dB	**Gain**= 11b, **Gain_ST3** = 000b
		12			dB	**Gain** = 00b, **Gain_ST3** = 000b
Gstep	Gain step		3		dB	**AGCEN** = 1
			12		dB	**AGCEN** = 0 Defined by **Gain[1:0]**
RxNoise	Intrinsic input referred noise in Rx		TBD		mVrms	

(1) CLoad : Load capacitance at **VMID** pin

Table 3-7: Operation Timing

Parameter	Description	Min	Typ	Max	Unit	Conditions
TPowerup	Startup time from Power up			4	mS	From Power up till system ready to receive commands
TstSPD	Startup time from Soft power down			1.8	mS	From Setting **Powerdown** = 0 until system ready to receive commands
TstHPD	Startup time from Hard power down			2.4	mS	From Setting **RSTPD** = 0 until system ready to receive commands
TstSTBY	Startup time from standby mode		0.5		uS	From Setting **Standby** = 0 until system ready to receive commands
TReload	Register Reload time		40		uS	
Ttune	Tuning Time		302		uS	

Table 3-8: EEPROM

Parameter	Description	Min	Typ	Max	Unit	Conditions
TEEprog	EEPROM programming time		4.9		mS	Programming 1 block
VddMinProg	Minimum Power supply for programming voltage	2.7			V	

Table 3-9: Regulator

Parameter	Description	Min	Typ	Max	Unit	Conditions
VREGIN	Regulator input voltage	4.5	5	7	V	
VREGOUT	Regulator output voltage	3.20	3.25	3.3	V	IREGOUT = 0 mA
IREGIN	Input regulator current			160	mA	
IREGOUT	Output regulator current			80	mA	
$\Delta Vout_{LineReg}$	Line regulation (ΔVout)		0.5	1	mV/V	IREGOUT = 0 mA , 4.5V < **VREGIN** < 7V
$\Delta Vout_{LoadReg}$	Load regulation (ΔVout)		0.25		mV/mA	**VREGIN** = 5 V , 0 < IREGOUT < 80 mA
VREGDrop	Drop Out Voltage			40	mV	IREGOUT = 80 mA
IREGBias	Regulator Bias Current	170	200	220	uA	5 V < **VREGIN** < 7 V

3.3 Support protocols

Table 3-10: Supported Protocols

Protocol	Transmitter		Receiver	
	Rate (kbps)	Coding	Rate (kbps)	Coding
ISO14443A	106, 212, 424, 848	Miller	106	Manchester
			212, 424, 848	BPSK
ISO14443B	106, 212, 424, 848	NRZ	106, 212, 424, 848	BPSK
ISO15693	26, 1.67	1 of 4, 1 of 256	53, 26, 13, 6.7	Manchester
			26, 13, 6.7	FSK
Crypto_M	106	Miller	106	Manchester

3.4 Peripheral Specification

Table 3-11: Peripheral Specification

Block	Properties	Min	Typ	Max	Unit
FIFO	Total Size		64		Byte
EEPROM	Total Size		256		Byte
	Write endurance	1,000,000			Time
	Retention	20			Years
Timer	Max time count		39.6		Sec
	Trigger source	TxStart, TxStop, RxStart, RxStop, User			-
Interrupt	Trigger source	Timer, Tx, Rx, Idle, FIFO, EEPROM			-
	Output Level	Toggle High, Toggle Low			-
Clock Divider	Output Frequency	13.56, 6.78, 3.39			MHz

3.5 Analog Characteristic

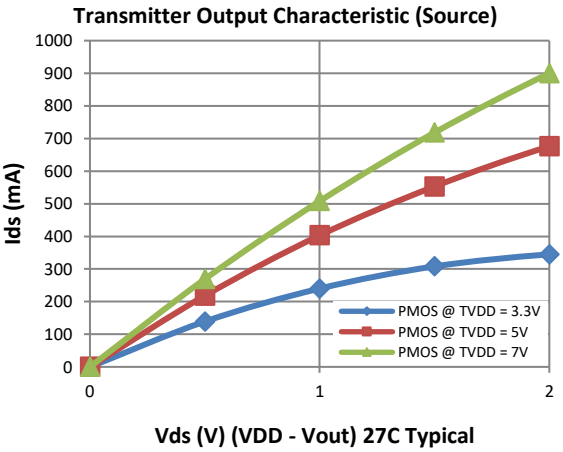


Figure 3-1: Transmitter source Characteristic

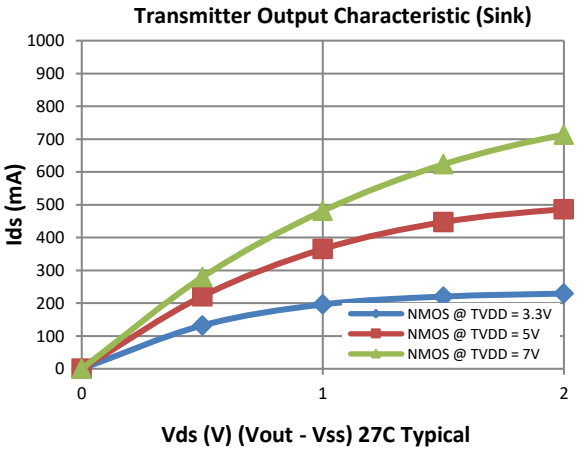


Figure 3-2: Transmitter sink Characteristic

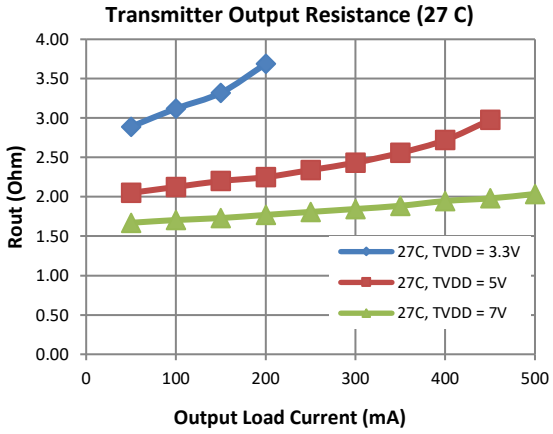


Figure 3-3: Transmitter Output Resistance at 27°C

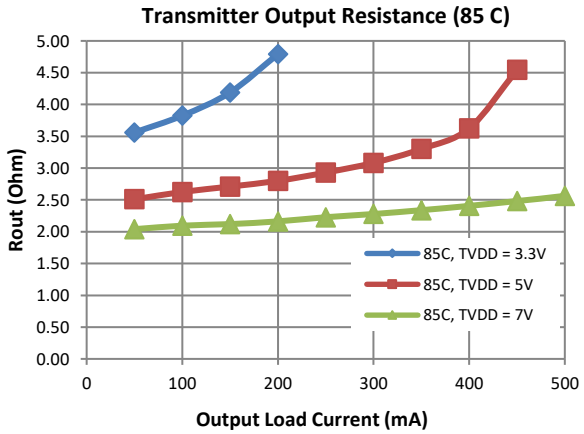


Figure 3-4: Transmitter Output Resistance at 85°C

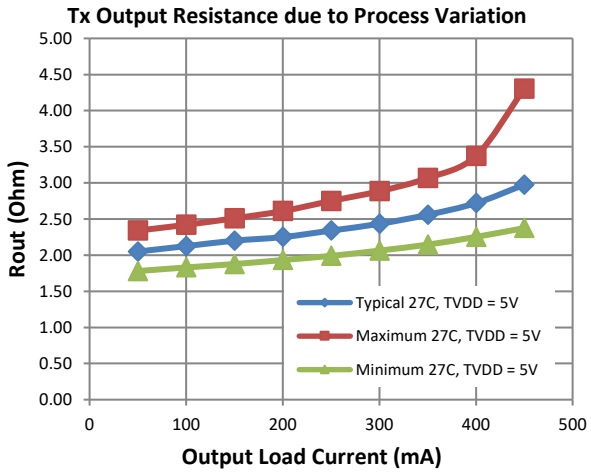


Figure 3-5: Maximum and minimum transmitter output Resistance

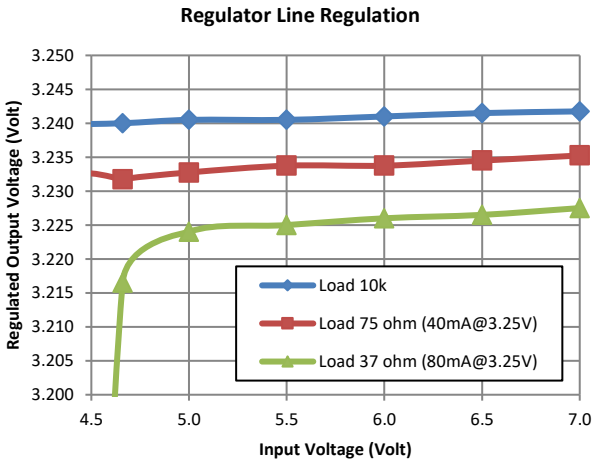


Figure 3-6: Regulator Line Regulation

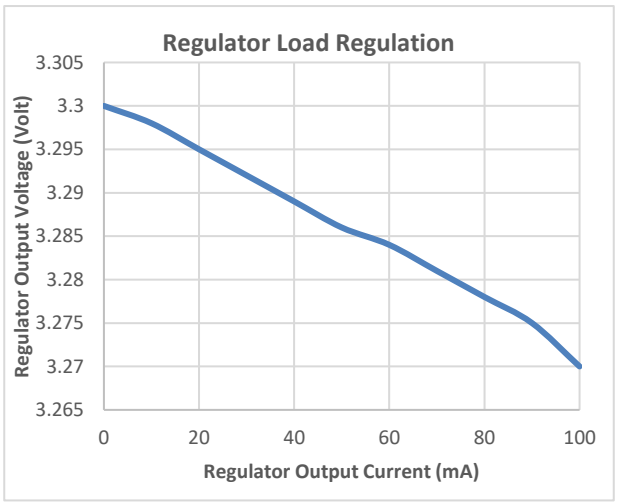


Figure 3-7: Regulator Load Regulation

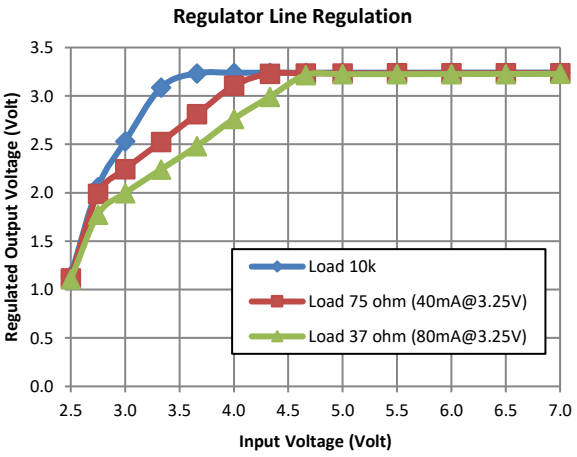


Figure 3-8: Regulator Transfer Characteristic

4. SPI Interface

The RE31 can be interfaced through a standard 4-wire SPI interface in order to access to internal registers. The SPI interface is capable of handling input stream up to 10 Mbps. There are 4 modes available where their timing diagrams are depicted in Figure 4-1 to Figure 4-4. Depending on activities of the interfacing controller, the purpose and usage of each SPI mode are shown in table below. The timing constrain is shown in Figure 4-5. Note that if NCS is set to high, MISO become high-impedance. This allows multiple SPI devices, in which Hi-Z feature in MISO available, controlled from the same MCU as shown in Figure 4-6.

Table 4-1: SPI Mode

Mode	Purpose and Usage
Single register/single byte write	Setting value from a single setting register
Single register/single byte read	Reading value from a single setting register
Single-register/multiple-byte write	Writing consecutive data to FIFO
Multiple-register/multiple-byte read	Reading consecutive data from FIFO. Monitoring status of RE31

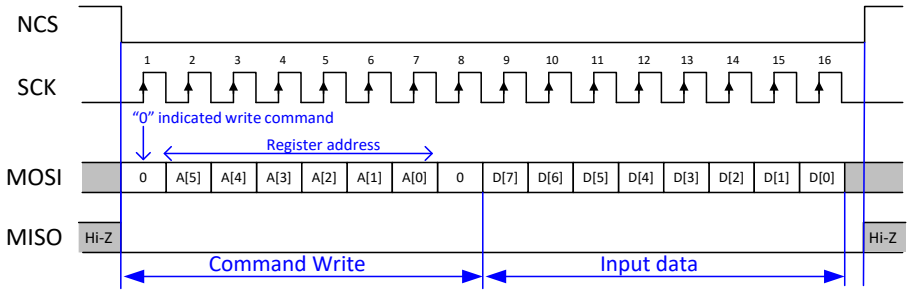


Figure 4-1: SPI interface for single register/single byte write

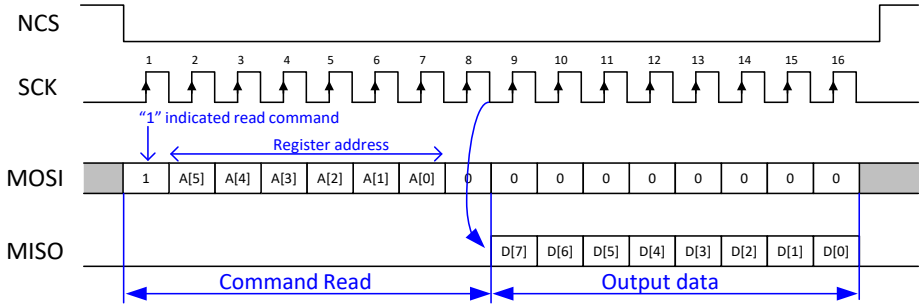


Figure 4-2: SPI interface for single register/single byte read

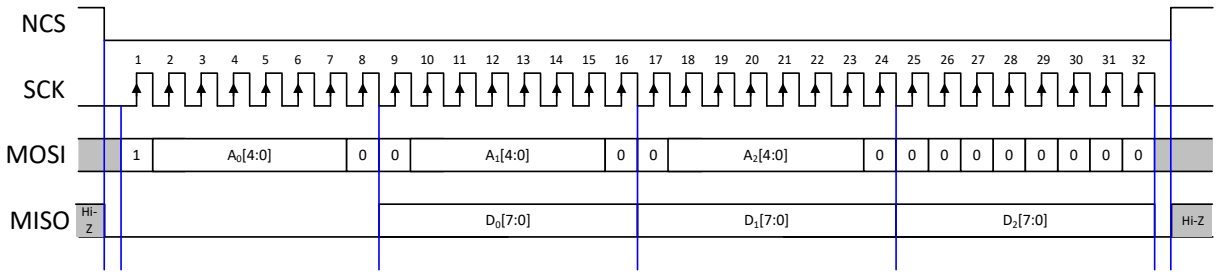


Figure 4-3: SPI interface for multiple-register/multiple-byte read

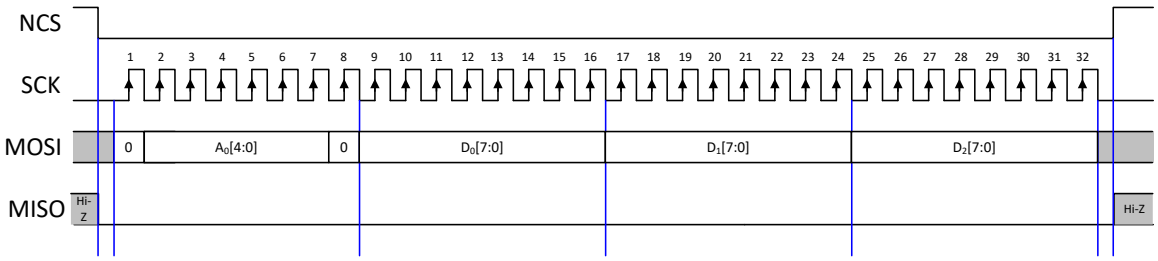


Figure 4-4: SPI interface for single-register/multiple-byte write

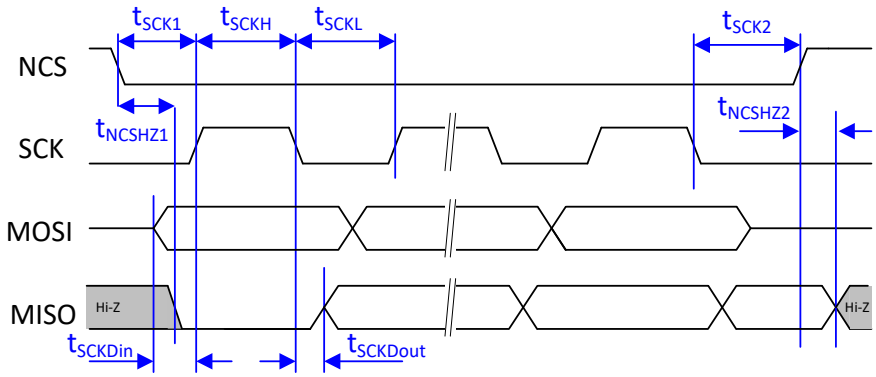


Figure 4-5: SPI timing interface

Table 4-2: SPI timing

Parameter	Description	Min	Max	Unit
tSCK1	NCS low to 1st SCK high	12		nS
tSCK2	Last SCK low to NCS high	12		nS
tSCKH	SCK high period	25		nS
tSCKL	SCK low period	25		nS
tSCKDin	Data change to SCK high	12		nS
tSCKDout	SCK low to data change	12		nS
tNCSHZ1	NCS low to MISO active	12		nS
tNCSHZ2	NCS High to MISO Hi-Impedance	12		nS
SPIclk	SPI clock		10	MHz

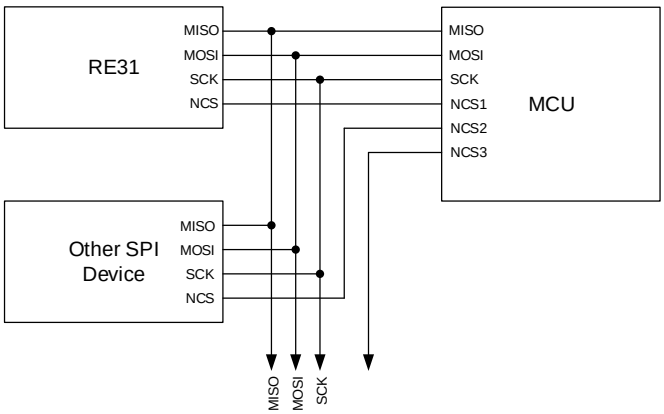


Figure 4-6: SPI interface to multiple SPI Devices having hi-Z feature in MISO output

5. Registers

5.1 Register Overview

The RE31 consists of 6-bit addressable registers grouped into 8 pages by their functions. There are 4 types of registers, namely Dynamic, Write only, Read/Write, Read only, in which their behaviours are described in Table 5-1. The overview of the registers is shown Table 5-2. The register names are listed in the far-right column, and the default values after reset are shown in the parenthesis. Note that "b" is omitted for the binary number of default value in Table 5-2.

Table 5-1: Type of Registers

Type	Description
Dynamic	The Dynamic register is used to control behaviours of the reader IC as wells as display the status. The Dynamic register can be either set by the external controller or automatically updated by the internal state machine.
Write only	The write-only register is used for control behaviours of the reader IC, especially timers and FIFO. These registers can only be written by the external controller. Reading from these registers returns zero.
Read/Write	The read-write register is used to configure and control behaviours of the reader IC. These registers can be written and read by the external controller.
Read only	The read only register is used to display the status of the internal state machine. Writing these registers will not affect their values.
Unused	These registers are intentionally left blank or reserved for future use.

Table 5-2: RE31 Register Map

Page		Addr		Bit 7	6	5	4	3	2	1	0	Register Name
Command and Status	0	0	0	RFU								RFU
		0	1	Command (0x00)								Command
		0	2	FIFOData								FIFO Data
		0	3		ModemState (000)			IRQ (0)	ERR (1)	HiAlert (0)	LoAlert (1)	Primary Status
		0	4	FIFO Length (0x00)								FIFO Length
		0	5	Trunning (0)	E2Ready (1)	CRCReady (1)	EMD_Det(0)	SubC_Det (0)	RxLastBits (000)			Secondary Status
		0	6	SetIEN (0)		TimerIEN (0)	TxIEN (0)	RxIEN (0)	IdleIEN (0)	HiAlertIEN (0)	LoAlertIEN(0)	Interrupt Enable
		0	7	SetIRq (0)		TimerIRq (0)	TxIRq (0)	RxIRq (0)	IdleIRq (1)	HiAlertIRq (0)	LoAlertIRq (1)	Interrupt Flag
Control and Status	1	0	8	RFU								RFU
		0	9			StandBy (0)	PowerDown (0)	Crypto_MOn(0)	TStopNow(0)	TStartNow(0)	FlushFIFO(0)	Control
		0	A	E2Err(0)	KeyErr(1)	AccessErr (0)	FIFOOvfl (0)	CRCErr (0)	FramingErr(0)	ParityErr(0)	CollErr(0)	ErrorFlag
		0	B	CollPos (0x00)								CollPos
		0	C	TimerValue (0xFF)								TimerValue
		0	D	CRCResultLSB (0x63)								CRCResultLSB
		0	E	CRCResultMSB (0x63)								CRCResultMSB
		0	F		RxAlign (000)				TxLastBits (000)			BitFraming
Tx and Coder	2	1	0	RFU								RFU
		1	1	Tx1Inv (0)	ModulatorSource (00)		Force100ASK(1)	Tx2Inv(1)	TX2Cw(0)	TX2RFEn(0)	TX1RFEn(0)	TxControl
		1	2			GsCfgCW (0x3F)						TxCfgCW
		1	3			GsCfgMod (0x28)						TxCfgMod
		1	4	Send1Pulse(0)		CoderRate (011)			TxCoding (001)			CoderControl
		1	5	ModWidth (0x0F)								ModWidth
		1	6	ModWidthSOF (0x0F)								ModWidthSOF
		1	7	NoTxSOF(0)	NoTxEOF(0)	EOFWidth(1)	CharSpacing (110)			SOFWidth (11)		TypeBFraming
Rx an Decoder	3	1	8	RFU								RFU
		1	9	SubCPulses (011)			SubCCarrier (01)		LP_Off (0)	Gain (11)		RxControl1
		1	A	RxMultiple(0)	CollMarkVal(0)	ZeroAfterColl(0)	RxFraming (01)			RxCoding (00)		DecoderControl
		1	B	BitPhase (0x3D)								BitPhase
		1	C	MinLevel (101)				CollLevel (101)				RxThreshold
		1	D	NoRx SOF (0)	NoRx EGT (0)	NoRx EOF (0)	HP2Off (0)	TauD (01)		AGC_EN (0)	TauAGC (0)	BPSKDemControl
		1	E	Cont_Int(0)	RxAutoPD (1)	VMidSel(0)	Reserve(0)	Reserve(0)	ByPassEnv(0)	Reserve(0)	DecoderSource(1)	RxControl2
		1	F	BPSKDecMeth(1)	BPSKDataRec(1)	SOFSel15693 (1)				EMD_Suppress(0)	SOFSel43A(0)	RxControl3
RF-Timming and Channel Redundancy	4	2	0	Page Select								Page Select
		2	1	Rx Wait (0x06)								RxWait
		2	2		MSBFirst(0)	CRC3309(0)	CRC8(0)	RxCRCEn(0)	TxCRCEn(0)	ParityOdd(1)	ParityEn(1)	ChannelRedundancy
		2	3	CRC Preset MSB (0x63)								CRCPresetMSB
		2	4	CRC Preset LSB (0x63)								CRCPresetLSB
		2	5									RFU
		2	6									RFU
		2	7									RFU
FIFO,Timer and IRQ-Pin Config	5	2	8	RFU								RFU
		2	9			Water_Level (0x08)						FIFOLevel
		2	A			TAutoRestart(0)	TPreScaler (00111)					TimerClock
		2	B					TStopRxEnd(0)	TStopRxBegin(1)	TStartTxEnd(1)	TStartTxBegin(0)	TimerControl
		2	C	TReloadValue(0A)								TimerReloadValue
		2	D									RFU
		2	E	M_HP1 (00)		M_LP1 (01)		M_HP2 (10)		M_LP2 (01)		ManualFilter
		2	F	Man_Filter(0)	EnAutoTune(1)			Filter_Corner_Coef (0101)				FilterAdjust
RFU	6	3	0	RFU								RFU
		3	1						CLKDIV_SEL(00)		IRQInv(0)	IOConfig
		3	2									RFU
		3	3									RFU
		3	4									RFU
		3	5									RFU
		3	6									RFU
		3	7	Signal Strength Indicator(SSI) (0000)				Corner_Frequency_Tuning_Value (CFTV)(XXXX)				Signal indicator
Test Control	7	3	8	RFU								RFU
		3	9									RFU
		3	A	IOMODE<1:0>(00)		Test<5:0>(000000)						Test
		3	B								Tx_Disable(0)	TxDisable
		3	C	Reserve (0x30)								Reserve1
		3	D	Reserve (0x00)								Reserve2
		3	E	Reserve (10101)					SP_Cyrpto(0)	Reserve (11)		Reserve3
		3	F	Reserve(00)		Gain_ST3 (000)			Reserved(001)			Gain_ST3

Legend ➔	R/W register	DY register	R register	W register	Analog/Digital register	Analog register	Digital register		

5.2 Register Details

5.2.1 Page 0 : Command and Status

Address	Name	Reset Value	Function
0x01	Command	0x00	Command execution register

Dy	dy	dy	dy	dy	dy	dy	dy
Command							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7:0	**Command**	Command register for executing RE31	
		Code	Command
		0x00	Idle
		0x1A	Transmit
		0x16	Receive
		0x1E	Transceive
		0x01	Write EEPROM
		0x03	Read EEPROM
		0x07	Load Config E2
		0x12	Calculate CRC
		0x0B	LoadKeyEEPROM
		0x19	LoadKeyFIFO
		0x1C	Authent
		0x10	Tune Filter

Address	Name	Reset Value	Function
0x02	FIFOData	0xXX	Input and output channel for 64-byte FIFO

dy	dy	dy	dy	dy	dy	dy	dy
FIFOData							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**FIFOData**	Input and output channel for transmission, reception, EEPROM data, and key initialization

Address	Name	Reset Value	Function
0x03	Primary Status	0x05	Flag for indicating the status of timer, modem, interrupt, and FIFO

	r	r	r	r	r	r	r
	ModemState			IRQ	ERR	HiAlert	LoAlert
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
6:4	**Modemstate**	ModemState shows states of RX, TX and, FIFO	
		000 : Idle	No Operation; Neither the transmitter nor the receiver is in operation
		001 : TxSOF	The transmitter is transmitting 'Start Of Frame' pattern
		010 : TxData	The transmitter is transmitting data from FIFO or CRC
		011 : TxEOF	The transmitter is transmitting 'End Of Frame' pattern
		100 : RxPrepare	Receiver circuitry is initialized at this state and wait for time period defined by *RxWait* and *Bitphase* before starting to receive data.
		101 : RxAwait	The receiver starts and is waiting for Rx Start of Frame from tag.
		110 : Receiving	The receiver is receiving data
3	**IRQ**	If there are one or more interrupt requests, the **IRQ** flag is set to 1.	
2	**ERR**	If one or more errors occur in the **Error** register (0x0A), the **ERR** flag is set to 1.	
1	**HiAlert**	If **FIFOlength** ≥ 64-**Waterlevel**, the **HiAlert** flag is set to 1.	
0	**LoAlert**	If **FIFOlength** ≤ **Waterlevel**, the **LoAlert** flag is set to 1.	

Address	Name	Reset Value	Function
0x04	FIFOLength	0x00	The FIFO length indicates the number of data remaining in the FIFO buffer.

R	r	r	r	r	r	r	r
FIFOLength							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**FIFOLength**	The FIFO length indicates the number of data remaining in the FIFO buffer.

Address	Name	Reset Value	Function
0x05	Secondary Status	0x60	Status Flag and Value related to Timer, EEPROM, CRC, and receiver status.

R	r	r			r	r	r
Trunning	E2Ready	CRCReady	EMD_Det	SubC_Det	RxLastBit		
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7	**Trunning**	If Timer is running, **Trunning** is set to 1. The value in **Timer Value** register decreases at the rate of timer clock, prescaling from 13.56 MHz by **TPreScaler.**
6	**E2Ready**	**E2Ready** being set to 1 indicates that the EEPROM has finished operation, i.e. programming or reading process. The EEPROM is in idle state and ready to operate next command.
5	**CRCReady**	**CRCReady** being set to 1 indicates that the CRC co-processor is in idle state and ready to operate.
4	**EMD_Det**	The **EMD_Det** is set to 1, if the reader system suppresses a frame that falls in EMD criteria. This indicator bit is active when control bit **EMD_Suppress** (0x1F.1) is enabled and is automatically cleared during "***RxAwaiting***" state.
3	**SubC_Det**	The **SubC_Det** is set to 1 when preamble or SOF is detected. In case of BPSK coding, **SubC_Det** asserts when preamble is detected. In case of Manchester and FSK coding, **SubC_Det** assert when SOF is detected. This bit is automatically cleared during *"**RxAwaiting**"* state.
2:0	**RxLastBit**	**RxLastBit** displays the number of valid bits in the last received byte in the bit-oriented frame response. If **RxLastBit** is zero, the last receiving byte is complete and valid.

Address	Name	Reset Value	Function
0x06	Interrupt Enable	0x00	Interrupt Enable Register

w		r/w	r/w	r/w	r/w	r/w	r/w
SetIEN		TimerIEn	TxIEn	RxIEn	IdleIEn	HiAlertEn	LoAlertEn
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7	**SetIEN**	**SetIEn** is a mask bit used in setting and resetting interrupt enable bits. Setting to 1 makes the interrupt enable bits, which are written with 1, set. Setting to 0 makes the interrupt enable bits, which are written with 1, cleared. Ex. Writing 3F to the interruptEn register clears all interrupt enable bits. Writing BF to the interruptEn register sets all interrupt enable bits.
6	-	-
5	**TimerIEn**	Set to 1, the timer interrupt request (TimerIRq) is sent to pin IRQ.
4	**TxIEn**	Set to 1, the transmitter interrupt request (TxIRq) is sent to pin IRQ.
3	**RxIEn**	Set to 1, the receiver interrupt request (RxIRq) is sent to pin IRQ.
2	**IdleIEn**	Set to 1, the idle interrupt request (IdleIRq) is sent to pin IRQ.
1	**HiAlertEn**	Set to 1, the FIFO HiAlert interrupt request (HiAlertIRq) is sent to pin IRQ.
0	**LoAlertEn**	Set to 1, the FIFO LoAlert interrupt request (LoAlertIRq) is sent to pin IRQ.

Address	Name	Reset Value	Function
0x07	Interrupt Request	0x05	Interrupt Request Register

w		dy	dy	Dy	dy	dy	dy
SetIRq		TimerIRq	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7	**SetIRq**	**SetIRq** is a mask bit used in setting and resetting interrupt request bits. Setting to 0 makes the interrupt request bits, which are written with 1, cleared. Setting to 1 has no effect. Ex. Writing 3F to the interruptEn register clears all interrupt request bits.
6	-	-
5	**TimerIRq**	**TimerIRq** is set to 1 when the timer value decreases to zero.
4	**TxIRq**	**TxIRq** is set to 1 when one of these events occurs : - *Transmit* Command : All data transmitted. - *Transceive* Command : All data transmitted. - *WriteE2* Command : All data programmed. - *CalCRC* Command : All data processed. - *Tuning* Command : Tuning process finished. - *LoadKeyEEPROM* : Key is already in the buffer. - *LoadKeyFIFO* : Key is already in the buffer.
3	**RxIRq**	**RxIRq** is set to 1 when the receiver finishes receiving, which can be one of these events. - *Transceive* Command : All data received. - *Receiver* Command : All data received.
2	**IdleIRq**	**IdleIRq** is set to 1 when the operation of command is finished and the state is changed to idle.End of operation of all commands causes **IdleIRq** set to 1. Setting power down, standby or *Idle command* does not set **IdleIRq**.
1	**HiAlertIRq**	**HiAlertIRq** is set to 1 when **FIFOlength** > 64 - Water_Level.
0	**LoAlertIRq**	**LoAlertIRq** is set to 1 when **FIFOlength** < Water_Level.

5.2.2 Page 1 : Control and Status

Address	Name	Reset Value	Function
0x09	Control	0x00	Control flag for all Operation of reader system

		dy	dy	Dy	w	w	W
-	-	StandBy	PowerDown	Crypto_MOn	TStopNow	TStartNow	FlushFIFO
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7	-	-
6	-	-
5	**StandBy**	Setting this bit to 1 enters the standby mode. The oscillator is still running. All current consuming blocks are turned off.
4	**PowerDown**	Setting this bit to 1 enters the software power down mode. The oscillator is turned off and all current consuming blocks are turned off.
3	**Crypto_MOn**	If **Crypto_MOn** is set to 1, the crypto engine is switched on and the RF communication is encrypted. Crypto_M is set to 1 only if the authentication process is successful. Crypto_M can be clear from external control.
2	**TStopNow**	Setting this bit to 1 stops the timer immediately. Reading result from this bit is always 0.
1	**TStartNow**	Setting this bit to 1 starts the timer immediately. Reading result from this bit is always 0.
0	**FlushFIFO**	If set to 1, the FIFO read/write-pointer and the **FIFOovlf** flag are cleared as well as the **FIFOlength** becomes zero. Reading result from this bit is always 0.

Address	Name	Reset Value	Function
0x0A	ErrorFlag	0x40	Error flag for a last executed command

r	r	r	r	R	r	r	r
E2Err	KeyErr	AccessErr	FIFOOvf	CRCErr	FrameErr	ParityErr	CollErr
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7	**E2Err**	**E2Err** is set to 1, if the EEPROM programming is not successful, e.g., erase errors from low supply voltage.
6	**KeyErr**	**KeyErr** is set to 1, if the key format in the key buffer is incorrect. Because the key buffer is not initialized, **KeyErr** is set after reset.
5	**AccessErr**	**AccessErr** is set to 1, if accessing to the forbidden area, e.g., reading EEPROM in the area that key is stored (write-only) or writing EEPROM in read-only.
4	**FIFOOvf**	**FIFOOvf** is set to 1, if FIFO is written from the external microprocessor or the state machine while FIFO is full. **FIFOOvf** is cleared when FIFO is flushed.
3	**CRCErr**	**CRCErr** is set to 1, if **RxCRCEn** is set, and the comparison between received CRC and calculated CRC giving a mismatched result. **CRCErr** is automatically cleared to 0 every time the receiver starts to receive.
2	**FrameErr**	**FramingErr** is set to 1, if the received frame format is not conformed to the defined protocol. **FramingErr** is automatically cleared to 0 every time the receiver starts to receive.
1	**ParityErr**	**ParityErr** is set to 1, if the parity check has failed. **ParityErr** is automatically cleared to 0 every time the receiver starts to receive.
0	**CollErr**	**CollErr** is set to 1, if the bit-collision in ISO14443A and ISO15693 is detected. **CollErr** is automatically cleared to 0 every time the receiver starts to receive.

Address	Name	Reset Value	Function
0x0B	Collision Position	0x00	Bit collision position

r	r	r	r	R	r	r	r
CollPos							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**CollPos**	**CollPos** indicates the bit position of the first detected collision in a received frame. **CollPos** supports ISO14443A Manchester coding and ISO15693. 0x00 indicates the bit collision which occurs at the start bit. 0x01 indicates the bit collision which occurs at the 1st bit. 0x0A indicates the bit collision which occurs at the 10th bit.

Address	Name	Reset Value	Function
0x0C	TImerValue	0xFF	Timer Value

r	r	r	r	R	r	r	r
TimerValue							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**TimerValue**	The value of the timer counter

Address	Name	Reset Value	Function
0x0D	CRCResultLSB	0x63	CRC Result

r	r	r	r	R	r	r	r
CRCResultLSB							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**CRCResultLSB**	The least significant byte of the result CRC. It is valid only if the bit *CRCReady* is set to 1.

Address	Name	Reset Value	Function
0x0E	CRCResultMSB	0x63	CRC Result

r	r	r	r	R	r	r	r
CRCResultMSB							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**CRCResultMSB**	The most significant byte of the result CRC. It is valid only if the bit *CRCReady* is set to 1.

Address	Name	Reset Value	Function
0x0F	Bit Framing	0x00	Bit Framing input/output for the transmission/reception of the bit-oriented frame.

	dy	dy	dy		dy	dy	dy
	RxAlign				TxLastBits		
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
6:4	RxAlign	RxAlign is used to define the position of the first received data bit to be stored in the first received byte in the bit oriented frame in ISO14443A. RxAlign is automatically cleared after the reception has finished in transceive and receive commands.
2:0	TxLastBits	TxLastBits is used to define the number of bits of the last byte to be transmitted in the bit oriented frame in ISO14443A. The value “000” is used to define the whole last bit that will be transmitted. TxLastBits is automatically cleared after the transmission has finished in transceive and transmit commands.

5.2.3 Page 2 : Tx and Coder

Address	Name	Reset Value	Function
0x11	TxControl	0x18	Control the logical behaviour of the transmitter driver on pin TX1, TX2

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Tx1Inv	Modulator Source		100ASK	Tx2Inv	Tx2Cw	Tx2RFEn	Tx1RFEn
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7	Tx1Inv	If set to 1, Tx1 will deliver an inverted 13.56-Mhz carrier.	
6:5	Modulator Source	Select Source for Coder input	
		00	Tri-state
		01	High
		10	Internal Coder
		11	Pin **SIGIN[0]**
4	100ASK	Setting this bit to 1 forces a 100% ASK Modulation, independent from the **CwConductance** value in the register 0x13. For ISO14443A and ISO15693 (100% modulation index), this bit should be set to 1.	
3	Tx2Inv	If set to 1, Tx2 will deliver an inverted 13.56-MHz carrier.	
2	Tx2Cw	If set to 1, Tx2 will continuously deliver an un-modulated 13.56-MHz carrier. If set to 0, Tx2 will deliver a modulated 13.56-MHz carrier.	
1	Tx2RFEn	If set to 1, Tx2 will deliver a 13.56-MHz carrier. If set to 0, Tx2 will drive a constant following Tx2Inv.	
0	Tx1RFEn	If set to 1, Tx1 will deliver a 13.56-MHz carrier. If set to 0, Tx1 will drive a constant following Tx1Inv.	

Address	Name	Reset Value	Function
0x12	TxCfgCW	0x3F	Configure TX1 and TX2 output conductance in the un-modulation state

		r/w	r/w	r/w	r/w	r/w	r/w
		TxCfgCW					
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	TxCfgCW	Define TX1 and TX2 output conductance in the un-modulation state field.

Address	Name	Reset Value	Function
0x13	TxCfgMod	0x28	Configure TX1 and TX2 output conductance in the modulation state

		r/w	r/w	r/w	r/w	r/w	r/w
		TxCfgMod					
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	TxCfgMod	Define TX1 and TX2 output conductance to regulate the output power during the modulation state (low level field). If Force100ASK is set to 1, the value of GsCfgMod has no effect.

Address	Name	Reset Value	Function
0x14	CoderControl	0x19	Set the coder rate and the coding mode

r/w		r/w	r/w	r/w	r/w	r/w	r/w
Send1Pulse		CoderRate			TxCoding		
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7	Send1Pulse	Setting this bit to 1 forces a generation of the only one modulation pulse to switch to the next TimeSlot in conjunction with an Inventory command in ISO 15693. This bit is not cleared automatically; it has to be reset to 0 by the user.	
5:3	CoderRate	Defined CoderRate	
		000	848kB for 14443A
		001	424kB for 14443A , 848KB for 14443B
		010	212kB for 14443A , 424KB for 14443B
		011	106kB for 14443A , 212KB for 14443B
		100	106KB for 14443B,
		101	ISO15693
		110	-
		111	-
2:0	TxCoding	Bit coding and Framing during Transmission	
		000	NRZ for 14443B
		001	Miller Coded for 14443A
		010	RFU
		011	RFU
		100	RFU
		101	RFU
		110	ISO15963 standard mode (1 out of 256 Coding)
		111	ISO15963 fast mode (1 out of 4 Coding)

Address	Name	Reset Value	Function
0x15	ModWidth	0x0F	Set the modulation pulse width

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
ModWidth							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	ModWidth	Define the pulse width of the modulation pulse in the transmitted bit. Modulation width = 2(ModWidth+1)/fc ISO14443A@106k : 0x0F (Modulation width = 2.36 us) ISO15693 : 0x3F (Modulation width = 9.44 us) This register is not affected if TxCoding is set to NRZ 14443B

Address	Name	Reset Value	Function				
0x16	ModWidthSOF	0x0F	Set the modulation pulse width in SOF				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
ModWidthSOF							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	ModWidth	Define the pulse width of the modulation pulse in Start of Frame in the transmitted telegram. Modulation width = 2(ModWidthSOF +1)/fc. For example, ISO14443A : 0x0F (Modulation width in SOF = 2.36 us). ISO 15693: 0x3F (Modulation width in SOF = 9.44 us). This register is not affected if TxCoding is set to NRZ 14443B.

Address	Name	Reset Value	Function				
0x17	TypeBTxFraming	0x3B	Define framing for ISO14443B transmission				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
NoTxSOF	NoTxEOF	EOFWidth	EGT			SOFWidth	
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7	NoTxSOF	If set to 1, the SOF will be omitted from the transmitted framing	
6	NoTxEOF	If set to 1, the EOF will be omitted from the transmitted framing	
5	EOFWidth	Set length of EOF	
		0	10 ETU
		1	11 ETU
4:2	EGT	Set length of the EGT length between 0 and 7 ETU when transmitted	
1:0	SOFWidth	Define SOF patterns in ISO14443B	
		00	10 ETU low and 2 ETU high
		01	10 ETU low and 3 ETU high
		10	11 ETU low and 2 ETU high
		11	11 ETU low and 3 ETU high

5.2.4 Page 3 : Rx and Decoder

Address	Name	Reset Value	Function
0x19	RxControl1	0x6B	Control receiver behaviours

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
SubCPulses			SubCCarrier		LPOff	Gain	
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7:5	**SubCPulses**	Define the number of subcarrier pulses per Bit.	
		000	1 Pulse (ISO14443A & 43B @848k)
		001	2 Pulses (ISO14443A & 43B @424k)
		010	4 Pulses (ISO14443A & 43B @242k)
		011	8 Pulses (ISO14443A & 43B @106k , ISO15693 @ 53k)
		100	16 Pulses (ISO15693 @ 26k, ICODE1)
		101	32 Pulses (ISO15693 @ 13k)
		110	64 Pulses (ISO15693 @ 6.7k)
		111	RFU
4:3	**SubCCarrier**	Define the number of carriers in the subcarrier.	
		00	8 Clks
		01	16 Clks (ISO14443A & ISO14443B)
		10	32 Clks (ISO15693)
		11	64 Clks
2	**Lp_Off**	Switch off all Lowpass filters to extend the incoming signal bandwidth.	
1:0	**Gain**	Define Gain of the Amplifier manually when the AGC is turned off (AGCEn is set to 0).	
		00	12 dB (4x)
		01	24 dB (16x)
		10	36 dB (64x)
		11	48 dB (250x)

Address	Name	Reset Value	Function
0x1A	DecoderControl	0x08	Control Decoder behaviours

r/w	r/w	r/w	r/w	r/w		r/w	r/w
RxMultiple	CollMarkVal	ZeroAfterColl	RxFraming			RxCoding	
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7	**RxMultiple**	If set to 1, system can receive consecutive reception without issuing ***Receive*** command. Every received data and its associated error register value, even if there is no error, are saved to FIFO. Every end of reception, *Rx interrupt* is asserted. To quit the reception, ***Idle*** command must be issued to the **Command** register. This command is applicable for both ***Transceive*** and ***Receive*** command.	
6	**CollMarkVal**	If set to 1, the collided bit is set to the value defined by CollMarkValue. This feature helps resolving anti-collision procedure for ISO14443A.	
5	**ZeroAfterColl**	If set to 1, all received bits after the collided bit are marked to zero. Otherwise, the data are recorded as decoder received. This feature eases resolving anti-collision procedure for ISO14443A.	
4:3	**RxFraming**	Define Decoder Framing.	
		00	RFU
		01	ISO 14443A
		10	ISO 15693, I-CODE2-SLI
		11	ISO 14443B
2	**-**	-	
1:0	**RxCoding**	Define receiving patterns for the decoder.	
		00	Manchester (ISO 14443A - 106 kbps , ISO 15693 – 1 subcarriers)
		01	BPSK (ISO 14443A - higher rate : 212, 424, 848kbps, and ISO 14443B)
		10	FSK (ISO 15693 – 2 subcarriers)
		11	RFU

Address	Name	Reset Value	Function
0x1B	BitPhase	0x3D	Define the phase relation between TX EOF and RX SOF

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
BitPhase							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**BitPhase**	Define the fractional guard time of the decoder in the clock unit. This register should be set in addition to **RxWait**, which is used for starting. Note: The correct value of this register is essential for proper operation.

Address	Name	Reset Value	Function
0x1C	RxThreshold	0xAA	Define a threshold of the bit decoder from the correlator

r/w	r/w	r/w		r/w	r/w	r/w	
MinLevel				Collevel			
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7:5	**MinLevel**	Define the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is evaluated as an invalid bit. The signal strength is relatively measured to the following working ranges. (8 steps in the design).	
		000	2/72 of Vdd
		001	3/72 of Vdd
		010	4/72 of Vdd
		011	5/72 of Vdd
		100	6/72 of Vdd
		101	7/72 of Vdd
		110	8/72 of Vdd
		111	9/72 of Vdd
4	-	-	
3:1	**Collevel**	Define the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester and FSK-coded signal to generate the bit-collision, which is relative to the amplitude of the stronger half-bit. (8 steps in design).	
		000	1/9 of stronger bit
		001	2/9 of stronger bit
		010	3/9 of stronger bit
		011	4/9 of stronger bit
		100	5/9 of stronger bit
		101	6/9 of stronger bit
		110	7/9 of stronger bit
		111	8/9 of stronger bit
0	-	-	

Address	Name	Reset Value	Function
0x1D	BPSKDemControl	0x04	Define Rx framing and decoding control for ISO14443B

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
NoRxSOF	NoRxEGT	NoRxEOF	HP2Off	TauDPLL		AGCEn	TauAGC
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7	**NoRxSOF**	If set to 1, a missing SOF will be ignored and no framing error reported. If set to 0, a missing SOF generates a framing error.	
6	**NoRxEGT**	If set to 1, the number of EGT not conforming to the standard will be ignored and no framing error reported.	
5	**NoRxEOF**	If set to 1, a missing EOF will be ignored and no framing error reported. If set to 0, a missing EOF generates a framing error.	
4	**HP2Off**	Switch off the 2nd high pass filter.	
3:2	**TauDPLL**	Define a time constant of the internal PLL during the data receiving phase.	
		00	4 pulses, lock-in 10 pulses
		01	8 pulses, lock-in 22 pulses
		10	16 pulses, lock-in 44 pulses
		11	32 pulses, lock-in 88 pulses
1	**AGCEn**	If set to 1, the amplifier gain is controlled by the AGC to establish the amplified output signal in a working range. If set to 0, the amplifier gain is defined by Gain [1:0].	
0	**TauAGC**	Define a time constant of the AGC.	
		0	Hi-Speed (1 Subcarrier) (The subcarrier is set by **Subcarriers** in the **RxControl1**)
		1	Lo-Speed (2 Subcarriers) (The subcarrier is set by **Subcarriers** in the **RxControl1**)

Address	Name	Reset Value	Function
0x1E	RxControl2	0x41	Additional Control decoder and source for receiver

r/w	r/w	r/w			r/w		r/w
Cont_Int	RxAutoPD	VMIDSel	Reserve	Reserve	ByPassEnv	Reserve	Decoder Source
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7	**Cont_Int**	If set to 1, the correlator gain in the receiver is boosted by 4X for ISO15693 low data rate (6.67kbps). If set to 0, the correlator gain equals 1.	
6	**RxAutoPD**	If set to 1, the receiver circuit is automatically switched on before receiving and switched off after receiving. This option can be used to reduce current consumption. If set to 0, the receiver is always activated.	
5	**VMidSel**	Select Reference for VMID	
		0	VDD/2 is selected for VMID. In this case, the input signal swing at Rx is limited to VDD-VSS rails
		1	VBG is set for VMID. The VBG reference might be required in high sensitivity and low noise applications. In this case, the input signal swing at Rx is limited to (2 x VMID).
4:3	**Reserve**	Reserve bits. These bits must be set to 0.	
2	**ByPassEnv**	Select types of analog input signals presenting at Rx pin for extended range applications.	
		0	Pin **Rx** receives a 13.56-MHz carrier-modulated signal (An Internal Envelope detector is employed).
		1	Pin **Rx** receives a carrier-demodulated signal (An Internal Envelope detector is bypassed).
1	**Reserve**	Reserve bits. These bits must be set to 0.	
0	**Decoder Source**	Select input signals for internal decoders (only for BPSK pattern).	
		0	External Signal through PIN **SIGIN[1].**
		1	Internal Demodulator.

Address	Name	Reset Value	Function				
0x1F	RxControl3	0xF0	Control receiver behaviours				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
BPSKDecMeth	BPSKDataRec	SOFSel15693	RFU	RFU	RFU	EMD_Suppress	SOFSel43A
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7	**BPSKDecMeth**	Define the BPSK Decoding Method. See detail in section 6.3.5.	
		0	Adaptive Framing.
		1	Digital Correlator.
6	**BPSKDataRec**	If set to 1, BPSK Data Recognition block is enabled. It improves BPSK data reception especially in case of noisy or antenna detuning. This option can be applied in ISO14443A higher rate and ISO14443B.	
		0	Disable
		1	Enable
5	**SOFSel15693**	Define the method of ISO15693 header recognition. If set to 1, system employ running window method to search for a matched pattern of 4 valid bits of SOF. If there is a combination pattern like SOF but contain some invalid bits, system continues to search for next valid SOF and is still in “Receiving” state. Else, if it is set to 0, system quits receiving state with error reports with this occurrence. This bit increases noise immunity in most cases. This option is recommended in both normal case and especially receiving write response in which response time is quite long and there is significant probability to find noise pattern similar to the SOF.	
		0	Disable
		1	Enable running window to search for SOF
1	**EMD_Suppress**	If set to 1, Enable EMD frame suppression. This option is applicable for ISO14443A and ISO14443B only. The condition for EMD suppression is that the number of data byte < 3 bytes and there is at least an error in reception frame. This frame will be neglected and not send to FIFO. See detail in section 7.4.5.	
0	**SOFSel43A**	Define the ISO14443A SOF condition.	
		0	Only 1 valid SOF bits will be sufficient condition to treat the incoming frame valid.
		1	At least consecutive 5 valid bits will be sufficient condition to treat the incoming frame valid. The 5 valid bits are SOF and 4-bits data.

5.2.5 Page 4 : RF-Timing and Channel Redundancy

Address	Name	Reset Value	Function
0x21	RxWait	0x06	Define the guard time from TX EOF to start receiving the timing for the receiver

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
RxWait							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**RxWait**	The RxWait defines the guard time between the Tx EOF and the start of receiving of the decoder in the unit of one-bit duration. This will increase receiving capability especially in noisy environment. The one-bit duration unit is defined from **SubCPulses** and **SubCCarrier** in the RxControl1 register. Ex. In ISO 14443A 106kbps, the RxWait should be set to 0x06.

Address	Name	Reset Value	Function
0x22	Channel Redundancy	0x03	Select the CRC and Parity check for receiving data

	r/w	r/w	r/w	r/w	r/w	r/w
MSBFirst	CRC3309	CRC8	RxCRCEn	TxCRCEn	ParityOdd	ParityEn
6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7	-	-
6	**MSBFirst**	If set to 1, MSB bit in data frame is the first bit used for CRC calculation.
5	**CRC3309**	If set to 1, the CRC-calculation is done according to ISO/IEC3309 for ISO 14443B and ISO 15693.
4	**CRC8**	If set to 1, the 8-bit CRC is calculated. If set to 0, the 16-bit CRC is calculated.
3	**RxCRCEn**	If set to 1, the last byte of the received frame is interpreted as the CRC byte. If set to 0, no CRC is expected at the end of the received frame.
2	**TxCRCEn**	If set to 1, the CRC is calculated for the transmitted frame and appended to end of the transmitted data. If set to 0, no CRC is appended and transmitted.
1	**ParityOdd**	If set to 1, the odd parity is calculated and compared with the received frame. If set to 0, ever parity is calculated and compared with the received frame.
0	**ParityEn**	If set to 1, the parity is inserted in the transmitted data stream at the end of each byte and expected in the received data stream (ISO 14443A). If set to 0, no parity bit is inserted or expected (ISO14443B and ISO15693).

Address	Name	Reset Value	Function
0x23	CRCPresetMSB	0x63	MSB of the 16-bit preset value of the CRC Register

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
CRCPresetMSB							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**CRCPresetMSB**	The most significant byte of the CRC preset value.

Address	Name	Reset Value	Function

0x24	CRC Preset LSB	0x63	LSB of the 16-bit preset value of the CRC Register				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
CRCPresetLSB							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**CRCPresetLSB**	The least significant byte of the CRC preset value

5.2.6 Page 5 : FIFOLevel, Timer and Analog filter Adjustment

Address	Name	Reset Value	Function
0x29	FIFOLevel	0x08	Define the level of FIFO for overflow and underflow warnings

		r/w	r/w	r/w	r/w	r/w	r/w
		Water Level					
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
5:0	**Water Level**	Define the level of FIFO for overflow and underflow warnings

Address	Name	Reset Value	Function
0x2A	TimerClock	0x07	Define the input clock to the timer and Control the timer reloading.

		r/w	r/w	r/w	r/w	r/w	r/w
		TAuto Restart	TPreScaler				
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
5	**TAutoRestart**	If set to 1, the timer automatically restarts and counts down from TReloadValue, instead of counting down to zero. If set to 0, the timer decrements to zero and the bit TimerIRq is set to 1.
4:0	**TPreScaler**	Define the timer clock, Ftimer. Tprescaler can be adjusted from 0 to 21. Ftimer = 13.56 MHz / ($2^{TPrescaler}$)

Address	Name	Reset Value	Function
0x2B	TimerControl	0x06	Setup automatic start and stop timers, triggered by events from RF.

				r/w	r/w	r/w	r/w
				Tstop RxEnd	Tstop RxBegin	Tstart TxEnd	Tstart TxBegin
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:4	-	-
3	**Tstop RxEnd**	If set to 1, the timer stops automatically after the end of data reception. If set to 0, the end of reception event does not affect the timer.
2	**Tstop RxBegin**	If set to 1, the timer stops automatically after the 1st valid bit is received. If set to 0, the reception of the 1st valid bit does not affect the timer.
1	**Tstart TxEnd**	If set to 1, the timer starts automatically after the end of transmission. If the timer is running, the timer restarts from TReloadValue. If set to 0, the end of transmission event does not affect the timer.
0	**Tstart TxBegin**	If set to 1, the timer starts automatically after the 1st valid bit is transmitted If the timer is running, the timer restarts from TReloadValue. If set to 0, the transmission of the 1st valid bit does not affect the timer.

Address	Name	Reset Value	Function
0x2C	TimerReloadValue	0x0A	Defined the timer start value

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
TReloadValue							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	**TReloadValue**	Define the timer start value. The value modification will affect the timer in the next round.

Address	Name	Reset Value	Function
0x2E	ManualFilter	0x19	Manual adjustment of the filter cut-off frequency r if the bit **Man_Filter** in the register **ManualFilterAdjust2** is set to 1.

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
M_HP1		M_LP1		M_HP2		M_LP2	
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7:6	**M_HP1**	Define high-pass cut-off frequency for the 1st stage high pass filter.	
		00	636 kHz
		01	318 kHz
		10	151 kHz
		11	75 kHz
5:4	**M_LP1**	Define low-pass cut-off frequency for the 1st stage low pass filter.	
		00	2400 kHz
		01	1200 kHz
		10	683 kHz
		11	363 kHz
3:2	**M_HP2**	Define high-pass cut-off frequency for the 2nd stage high pass filter.	
		00	381 kHz
		01	151 kHz
		10	75 kHz
		11	37 kHz
1:0	**M_LP2**	Define low-pass cut-off frequency for the 2nd stage low pass filter.	
		00	2400 kHz
		01	1200 kHz
		10	683 kHz
		11	363 kHz

Address	Name	Reset Value	Function				
0x2F	FilterAdjust	0x45	Filter corner adjustments				
r/w	r/w			r/w	r/w	r/w	r/w
Man_Filter	EnAutoTune			Filter_Corner_Coef			
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7	**Man_Filter**	If set to 1, the Filter corner is defined following the Manual Filter Control register. If set to 0, the Filter corner is defined by the Rx Mode.	
6	**EnAutoTune**	Select mechanism in tuning filter corners.	
		0	Filter tuning coefficient is configured through **Filter_Corner_Coef.**
		1	Filter tuning coefficient is configured by the tuning result from the tuning command.
5:4	-	-	
3:0	**Filter_Corner_Coef**	**Filter_Corner_Coef** defines the filter corner frequency. 0000 : The corner frequency is set to the highest adjustable value. 1111 : The corner frequency is set to the lowest adjustable value. 0101 : Default value.	

5.2.7 Page 6 : Clock Divider, IRQ-Pin, SSI and Tuning Value

Address	Name	Reset Value	Function
0x31	IO Configuration	0x00	IO configuration register

					r/w	r/w	r/w
					CLKDIV		IRQInv
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7:3	-	-	
2:1	**CLKDIV**	Define the frequency of the clock output at CLKBF pin for the external microcontroller or the digital system.	
		00	13.56 MHz
		01	6.78 MHz
		10	3.39 MHz
		11	0 MHz Low (No clock transmitted from CLKBF pin)
0	**IRQInv**	If set to 1, the IRQ pin is in active low.	

Address	Name	Reset Value	Function
0x37	Signal indicator	0xXX	Signal Strength Indicator and Corner Frequency tuning result

r	r	r	r	r	r	r	r
Signal Strength Indicator(SSI)				Cut-off Frequency Tuning Value (CFTV)			
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:4	**SSI**	Display subcarrier signal strength 0000 : 2 – 2.7 mV 0001 : 2.7 – 3.9 mV 0010 : 3.9 – 5.5 mV 0011 : 5.5 – 7.7 mV 0100 : 7.8 – 11 mV 0101 : 11 – 16 mV 0110 : 16 – 22 mV 0111 : 22 – 31 mV 1000 : 31 – 44 mV 1001 : 44 – 62 mV 1010 : 62 – 88 mV 1011 : 88 – 125 mV 1100 : 125 – 175 mV 1101 : 175 – 250 mV 1110 : 250 – 350 mV 1111 : 350 – 500 mV
3:0	**CFTV**	This register shows the result of tuning value after using command “tuning filter”. The tuning value affects all filters in receiver chain.

5.2.8 Page 7 : Test Control, Reserved, Gain_ST3

Address	Name	Reset Value	Function				
0x3A	Test	0x00	Register for test configuration				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
IOMODE<1:0>		Test<5:0>					
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:6	IOMODE	Define IO functionalities in the Test Mode.
5:0	Test	Test code to bring internal signals to test pads TA, TD0, TD1

IOMODE <1:0>	Function of Pins						Purpose
	CLKBF	IRQ	TD[0]	TD[1]	SIGIN[0]	SIGIN[1]	
00	CLKBF	IRQ	TD0	TD1	ENV_Ext*	Start_of_Rx_Ext**	Normal Mode
Other	Reserve for Test Mode						

* **ENV_Ext** is a modulation-control signal which is used only if a special modulation from an external source, e.g., MCU, is required.
** **Start_of_Rx_Ext** is an external bit codec-starting signal which is used in the test mode, and in case of employing receivers with only analog front end.

Address	Name	Reset Value	Function				
0x3B	TxDisable	0x00	Reserved				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
							Tx_Disable
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:1	Reserve	Reserved register for internal settings. For proper operation of the reader IC, do not modify the contents of this register different from reset value.
0	Tx_Disable	If set to 1, the Transmitter is disable. Tx control registers are forced as follows. Tx1RFEn = 0, Tx2RFEn = 0, Tx1Inv = 1,Tx2CW = 1, Tx2Inv = 1.

Address	Name	Reset Value	Function				
0x3C	Reserve1	0x30	Reserved				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reserve1							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	Reserve1	Reserved register for internal settings. For proper operation of the reader IC, do not modify the contents of this register different from reset value.

Address	Name	Reset Value	Function				
0x3D	Reserve2	0xXX	Reserved				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reserve2							
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:0	Reserve2	Reserved register for internal settings. For proper operation of the reader IC, do not modify the contents of this register different from reset value.

Address	Name	Reset Value	Function				
0x3E	Reserve3	0xAB	Encryption method				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reserve3					SP_Crypto	Reserve3	
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description
7:3	Reserve3	Reserved register for internal settings. For proper operation of the reader IC, do not modify the contents of this register different from reset value.
2	SP_Crypto	Define encryption method for authentication '0' : Crypto_M '1' : SP Crypto (SIC Proprietary crypto)
1:0	Reserve3	Reserved register for internal settings. For proper operation of the reader IC, do not modify the contents of this register different from reset value.

Address	Name	Reset Value	Function				
0x3F	GAIN_ST3	0x01	Gain of the last state amplifier				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reserve		Gain_ST3			Reserve		
MSB(7)	6	5	4	3	2	1	LSB(0)

Bit	Name	Function and Description	
7:6	Reserve	Reserved register for internal settings. Write this register with 00.	
5:3	Gain_ST3	Define gain of the last state amplifier for systems requiring extensive gain.	
		000	1 X (+ 0 dB)
		001	1.4 X (+ 3 dB)
		010	2 X (+ 6 dB)
		011	2.8 X (+ 9 dB)
		100	4 X (+ 12 dB)
		101	5.6 X (+ 15 dB)
		110	8 X (+ 18 dB)
		111	11 X (+ 21 dB)
2:0	Reserve	Reserved register for internal settings. Write this register with 000 or 001.	

5.3 Recommended Register Value for Normal operation

Table 5-3: Recommended Register value need to be set for each supported protocol

			Protocol	Default	43A				43B				15693 Tx		15693 Rx Man			15693 Rx FSK	
			Data Rate	/ Reset	106	212	424	848	106	212	424	848	1/4	1/256	53k	26k	6.7k	26k	6.7k
Page		Addr	Register Name																
Command and Status	0	0 1	Command	0x00															
		0 2	FIFO Data	0xXX															
		0 3	Primary Status	0x05															
		0 4	FIFO Length	0x00															
		0 5	Secondary Status	0x60															
		0 6	Interrupt Enable	0x00															
		0 7	Interrupt Flag	0x05															
Control and Status	1	0 9	Control	0x00															
		0 A	ErrorFlag	0x40															
		0 B	CollPos	0x00															
		0 C	TimerValue	0xFF															
		0 D	CRCResultLSB	0x63															
		0 E	CRCResultMSB	0x63															
		0 F	BitFraming	0x00															
Tx and Coder	2	1 1	TxControl	0x18	0x5B	0x5B	0x5B	0x5B	0x4B	0x4B	0x4B	0x4B	0x5B	0x5B					
		1 2	TxCfgCW	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F					
		1 3	TxCfgMod	0x28					0x10	0x10	0x10	0x10							
		1 4	CoderControl	0x19	0x19	0x11	0x09	0x01	0x20	0x18	0x10	0x08	0x2F	0x2E					
		1 5	ModWidth	0x0F	0x0F	0x07	0x02	0x01					0x3F	0x3F					
		1 6	ModWidthSOF	0x0F	0x0F	0x07	0x02	0x01					0x3F	0x3F					
		1 7	TypeBFraming	0x3B					0x3B	0x3B	0x3B	0x3B							
Rx an Decoder	3	1 9	RxControl1	0x6B	0x6B	0x4B	0x2B	0x0B	0x6B	0x4B	0x2B	0x0B			0x73	0x93	0xD3	0x93	0xD3
		1 A	DecoderControl	0x08	0x28	0x29	0x29	0x29	0x19	0x19	0x19	0x19			0x30	0x30	0x30	0x32	0x32
		1 B	BitPhase	0x3D	0x3D										0x88	0x40	0x0E	0x40	0x0E
		1 C	RxThreshold	0xAA	0x8C	0x88	0x44		0x88	0x88	0x44				0xAA	0xAA	0xAA	0xAA	0xAA
		1 D	BPSKDemControl	0x04	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02			0x02	0x02	0x02	0x02	0x02
		1 E	RxControl2	0x41	0x41	0x41	0x41	0x41	0x41	0x41	0x41	0x41			0x41	0x41	0x41	0x41	0x41
		1 F	RFU	-															
RF-Timming and Channel Redundancy	4	2 1	RxWait	0x06	0x07	0x07	0x07	0x07	0x03	0x03	0x03	0x03			0x10	0x08	0x02	0x08	0x02
		2 2	ChannelRedundancy	0x03	0x03	0x0F	0x0F	0x0F	0x2E	0x2E	0x2E	0x2E	0x2C	0x2C	0x2C	0x2C	0x2C	0x2C	0x2C
		2 3	CRCPresetLSB	0x63	0x63	0x63	0x63	0x63	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
		2 4	CRCPresetMSB	0x63	0x63	0x63	0x63	0x63	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
		2 5	RFU	-															
		2 6	RFU	0x00															
		2 7	RFU	-															
FIFO,Timer and IRQ-Pin Config	5	2 9	FIFOLevel	0x08															
		2 A	TimerClock	0x07															
		2 B	TimerControl	0x06															
		2 C	TimerReload	0x0A															
		2 D	RFU	-															
		2 E	Manual Filter Control	0x19															
		2 F	F-TuningControl	0x45															
RFU	6	3 1	IOConfig	0x00															
		3 2	RFU	-															
		3 3	RFU	-															
		3 4	RFU	-															
		3 5	RFU	-															
		3 6	RFU	-															
		3 7	Signal Indicator	0xXX															
Test Control	7	3 9	RFU	-															
		3 A	Test	0x00															
		3 B	Reserve	0x00															
		3 C	Reserve	0x30															
		3 D	Reserve	0xXX															
		3 E	Reserve	0xAB															
		3 F	Gain_ST13	0x01															

6. Architecture and Peripheral

6.1 Oscillator and Clock Divider

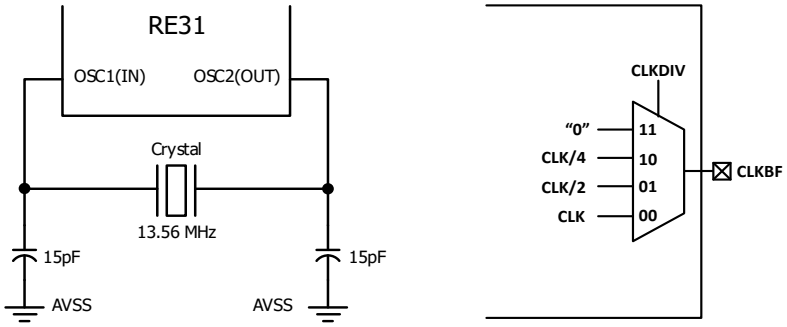


Figure 6-1: Crystal Oscillator and Clock Divider

The RE31 incorporates a stable low-jitter internal oscillator for generating a master clock for internal and external systems. The RE31 accepts self crystal oscillator and external clock feeding. In certain applications, e.g., long range readers where noise is a major limiting factor, employing an internal oscillator is recommended to obtain minimum jitter.

In case of external clock sources, following criteria must be taken into account.

- The duty cycle must be within 40% to 60%.
- The source should be stable and low jitter. The more jitter, the more noise in the RF system.
- The external clock must be fed to the oscillator input, pin **OSC1** .

To simplify the reader system, the RE31 provides a buffered clock driver for an external system in which frequency is selectable by the register **CLKDIV_SEL** (0x31.[2:1]) ranging from Clk, Clk/2,Clk/4 or turned-off.

6.2 Transmitter

A transmitter consists of two drivers and a control logic. The drivers are capable of operating from 2.7 V to 7 V from TVDD supply voltages separated from an analog core and a digital core. Wide operating supply voltages enable various applications from desktop to mid-range panel readers realized by a single RFID reader IC. The drivers are flexibly configured to connect to either closed-coupling matching networks or external drivers, e.g., class-E amplifiers in long range applications. The transmitter block diagram is shown in Figure 6-2.

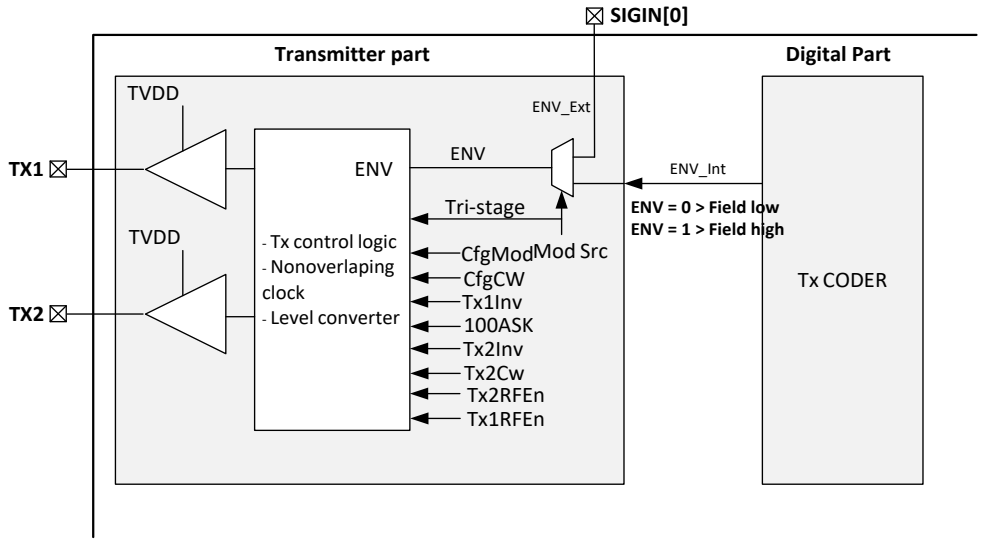


Figure 6-2: Simplified Transmitter System

The driving behaviour of the transmitter is defined by the register **TxControl** (0x11). By configuring registers **Tx1Inv, Tx2Inv**, **Tx2CW**, **Tx2RFEn,** and **Tx1RFEn**, the driver can provide a differential modulated output, a single-ended modulated output, or a plain carrier with a baseband signal for driving external circuitry. Setting **100ASK** makes the transmitter stops driving carrier during the modulation period. The behaviours of the transmitter in all possible combinations are shown in Table 6-1 and Table 6-2, for pin **`TX1`** and pin **`TX2`** respectively.

In case of an ASK modulation where the **100ASK** is reset, the conductance of the drivers is controlled by two 6-bit registers **TxCfgCW** (0x12) and **TxCfgMod** (0x13) to create two different RF levels, called un-modulation and modulation respectively. **TxCfgCW** corresponds to the level high of the baseband signal ***ENV*** from the transmitter coder, whereas **TxCfgMod** corresponds to the level low. Based on the transmitted signal from the coder, value of **TxCfgCW** must be higher than that of **TxCfgMod** to make the pattern of the RF-field modulation conform to the standard. Depending on the antenna characteristic, the modulation index can be adjusted from 0% to 60% with 63 steps resolution if **TxCfgCW** is set to the maximum value of 0x3F.

The transmitter is allowed to transmit data from an internal coder, an external control signal via pin **`SIGIN[0]`**, or a tri-state set through a register **Modulator Source**. The output driver incorporates a non-overlapping clock to reduce the power due to switching leakage current from TVDD to TVSS. Note that the logic of the signal ***ENV_Int*** from the coder in the rest state is high(1). Examples of **TxControl** configurations for various working modes are shown in Table 6-3 and Figure 6-3.

The bit modulation pattern and the frame format for the operating standards can be configured from the register **CoderControl** (0x14). Table 6-4 shows **CoderControl** settings for ISO14443A, ISO14443B, and ISO15693. In addition, the RF modulation width in both transmitted bits and the SOF in ISO14443A and ISO15693 can be adjusted from **ModWidth**(0x15) and **ModWidthSOF** (0x16) respectively at the resolution of 2 clocks. For ISO14443B, the transmitted frame format, related to SOF, EOF, and EGT, can be configured via the register **TypeBTxFraming** (0x17).

In addition, the output driver includes the non-overlapping clock to reduce the power due to leakage current from vdd to ground during switching.

Address	Name	Reset Value	Function				
0x11	TxControl	0x58	Control the logical behaviour of the transmitter driver on pin TX1, TX2				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Tx1Inv	Modulator Source		100ASK	Tx2Inv	Tx2Cw	Tx2RFEn	Tx1RFEn
MSB(7)	6	5	4	3	2	1	LSB(0)

Table 6-1: Tx1 Driver Behaviours on TxControl Combinations

Configuration			INPUT (*ENV_Int*)	Output		Mode
Tx1RFEn	100ASK	Tx1Inv		**TX1 Logic**	**TX1 Conductance**	
0	X	0	0	**0**	**Short to TVSS**	Shutdown or Connect to external Circuit
0	X	0	1	**1**	**CfgCWP**	
0	X	1	0	**1**	**CfgMODP**	Shutdown
0	X	1	1	**1**	**CfgCWP**	
1	0	0	0	**RF**	**CfgMODP**	Modulation 10-60% ASK
1	0	0	1	**RF**	**CfgCWP**	
1	0	1	0	**RF_N**	**CfgMODP**	
1	0	1	1	**RF_N**	**CfgCWP**	
1	1	0	0	**0**	**Short to TVSS**	Modulation 100% ASK
1	1	0	1	**RF**	**CfgCWP**	
1	1	1	0	**1**	**CfgCWP**	
1	1	1	1	**RF_N**	**CfgCWP**	

Table 6-2: Tx2 Driver Behaviours on TxControl Combinations

Configuration				INPUT (*ENV_Int*)	Output		Mode
Tx2RFEn	100ASK	TX2CW	Tx2Inv		**TX2 Logic**	**TX2 Conductance**	
0	X	0	0	0	**0**	**Short to TVSS**	Shutdown or Connect to external Circuit
0	X	0	0	1	**1**	**CfgCWP**	
0	X	0	1	0	**1**	**CfgMODP**	Shutdown
0	X	0	1	1	**1**	**CfgCWP**	
0	X	1	0	0	**0**	**Short to TVSS**	
0	X	1	0	1	**0**	**Short to TVSS**	
0	X	1	1	0	**1**	**CfgCWP**	
0	X	1	1	1	**1**	**CfgCWP**	
1	0	0	0	0	**RF**	**CfgMODP**	Modulation 10-60% ASK
1	0	0	0	1	**RF**	**CfgCWP**	
1	0	0	1	0	**RF_N**	**CfgMODP**	
1	0	0	1	1	**RF_N**	**CfgCWP**	
1	1	0	0	0	**0**	**Short to TVSS**	Modulation 100% ASK
1	1	0	0	1	**RF**	**CfgCWP**	
1	1	0	1	0	**1**	**CfgCWP**	
1	1	0	1	1	**RF_N**	**CfgCWP**	
1	X	1	0	X	**RF**	**CfgCWP**	CW on TX2 , carrier derived (connect to external circuit)
1	X	1	1	X	**RF_N**	**CfgCWP**	

Table 6-3: Suggested values and applications for transmitter configuration controls

Value	Mode	Tx1 Output	Tx2 Output	Purpose	Supported Standard
0x00	Shut down TX	Hi-Z	Hi-Z		
0x58	Shut down TX	1	1	Shut down	
0x4B	Differential Output, ASK	Modulated 13.56MHz carrier	Inverted modulated 13.56MHz carrier		ISO14443B, ISO15693,
0x43	Double Power, Single ended Output, ASK	Modulated 13.56MHz carrier	Modulated 13.56MHz carrier	Tx1 and Tx2 can be shorted together for double power	ISO14443B, ISO15693,
0x5B	Differential Output, 100%ASK	Modulated 13.56MHz carrier	Inverted modulated 13.56MHz carrier		ISO14443A, ISO15693
0x53	Double Power, Single ended Output, 100%ASK	Modulated 13.56MHz carrier	Modulated 13.56MHz carrier	Tx1 and Tx2 can be shorted together for double power	ISO14443A, ISO15693
0x46	Driving External circuitry	Internal Baseband sub-carrier signal	13.56 MHz carrier	Connect to the external driver, e.g., Class E Amplifier	ISO14443B, ISO15693

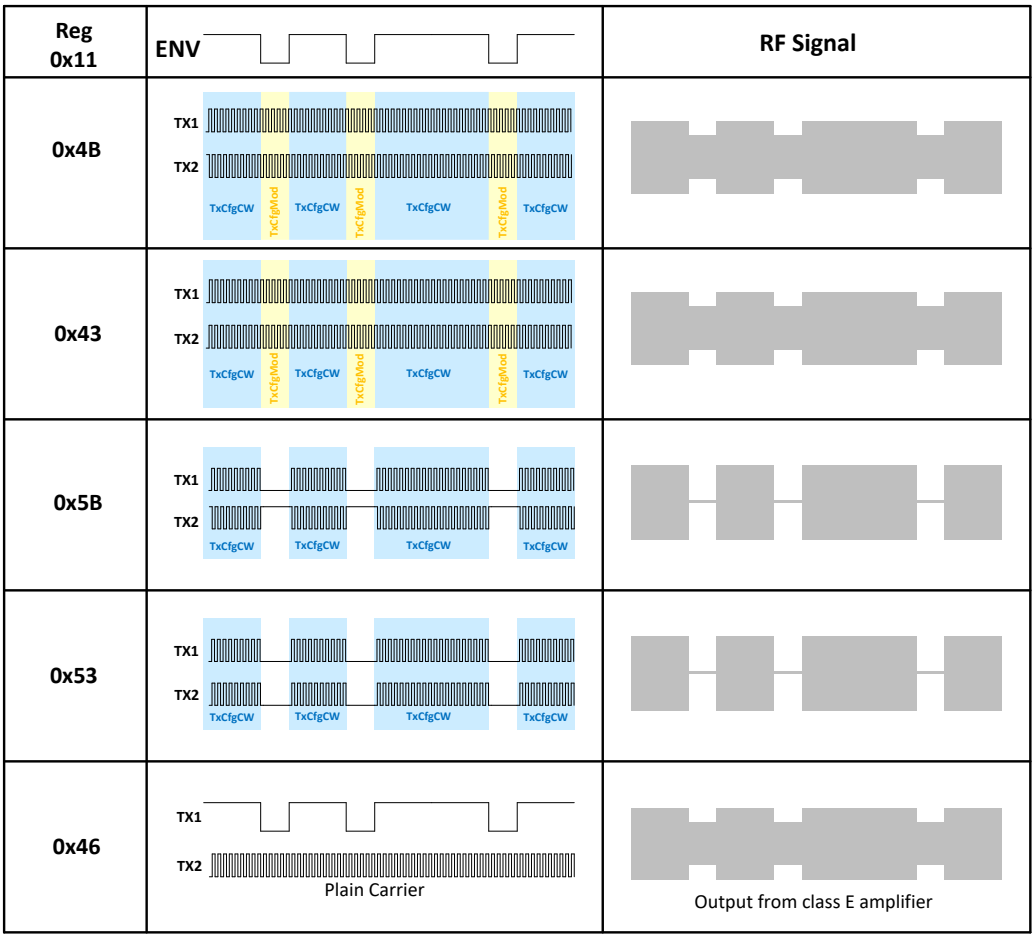


Figure 6-3: RF signal pattern and Output logic level during modulation

Table 6-4: CoderRate and TxCoding settings for supported standards

Standard	Tx Rate	CoderRate	TxCoding
ISO14443A	106 kbps	011	001
	212 kbps	010	001
	424 kbps	001	001
	848 kbps	000	001
ISO14443B	106 kbps	100	000
	212 kbps	011	000
	424 kbps	010	000
	848 kbps	001	000
ISO15693	1 of 4	101	110
	1 of 256	101	111

6.3 Receiver

The receiver part consists of an envelope detector, a voltage reference generator, an amplifier–filter system, a filter tuning system, a BPSK-bit decoder, a Manchester-and-FSK decoder, a Frame decoder, and a Timing control generator. The conceptual block diagram is shown in Figure 6-4.

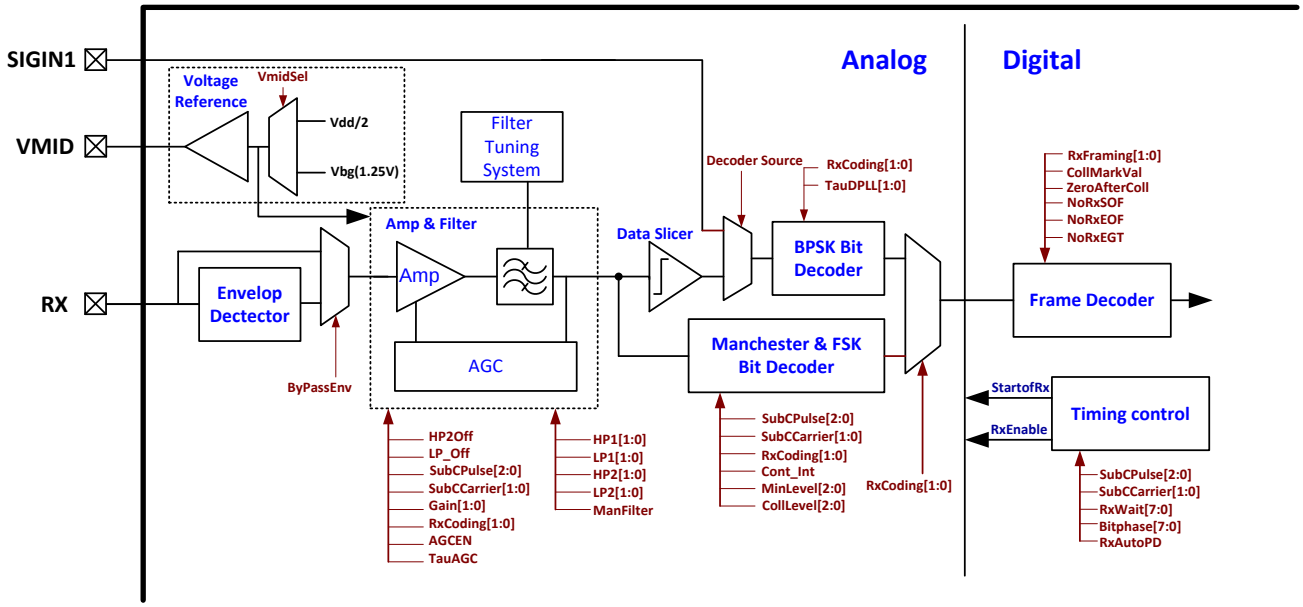


Figure 6-4: A Simplified Receiver System

6.3.1 Envelope detector

The RE31 embeds an internal envelope detector to extract the card-modulation signal from the RF carrier presented at pin ***RX***. The internal envelope detector is suitable for proximity readers. In addition, the RE31 architecture allows employing an external envelope detector to boost read range. In this case, the register **ByPassEnv** (0x1E.2) must be set to route the input signal directly to the filter-amplifier section. Depending on the selected voltage reference and bypass option, the maximum signal swings at pin ***RX*** for each configuration are shown in Figure 6-5. If the internal envelope detector is employed, the amplitude of the signal carrier at pin ***RX*** must be kept in rail-to-rail or 2.4 volt/gnd depending on VMID voltage selection. In case of external envelope detector, the input signal to the pin ***RX*** must be kept within 0.5 volt and VDD - 0.5 volt to prevent distortion.

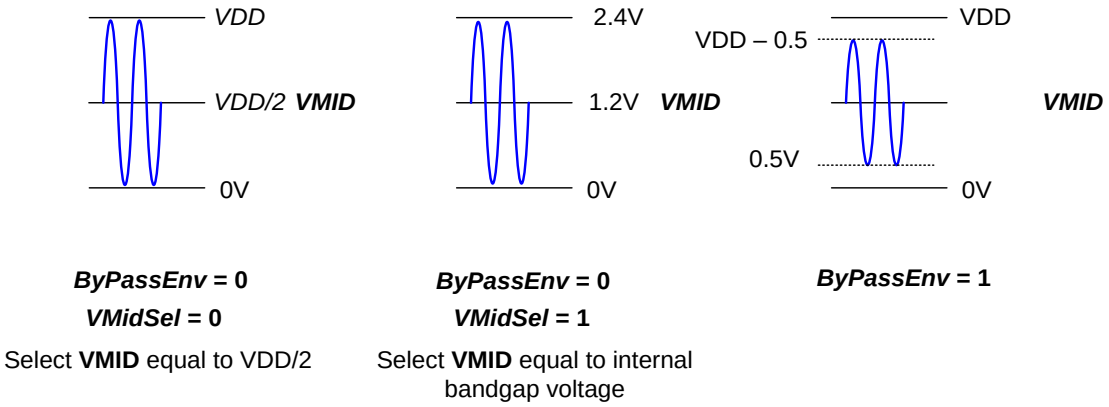


Figure 6-5: Signal swing at pin ***RX***

6.3.2 Voltage reference generator

The voltage reference generator provides a reference voltage for a receiver divider path through pin ***VMID***, and an internal voltage reference. The reference voltage can either be VDD/2 or 1.2-Volt bandgap. The selection can be made through the register **VMidSel** (0x1E.5). As shown in Figure 6-5, selecting VDD/2 is suitable for accepting a wide input strength from rail-to-rail at pin ***RX***, whereas the 1.2-volt bandgap is power-supply independent, suitable for low noise system, but the input signal swing is limited to 2.4 Volt.

6.3.3 An amplifier-filter system

The filter and the amplifier remove unwanted RF carriers, enlarge the received signal from the envelope detector, and reconstruct the baseband signal. The amplifier incorporates automatic gain control (AGC) to adjust the amplitude of the amplified baseband signal to a proper working range. Figure 6-6 shows detailed structures of the amplifier-filter system.

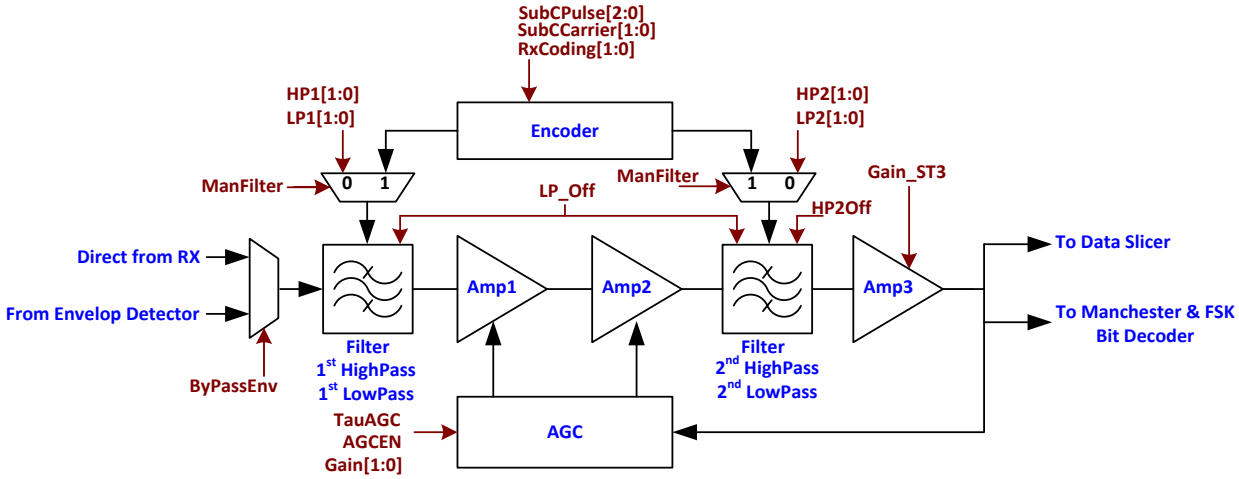


Figure 6-6: Detailed structures of an amplifier-filter system

Employing the AGC can discriminate the larger signal from the smaller signal in case of anti-collision for Manchester coding. As a result, the cards nearer to the reader will be seen first. Also, the AGC prevents the pulse shape from distortion, especially in BPSK coding. In addition, in noisy environment, the AGC adjusts the gain to the maximum operable value that the noise is not overwhelmed the internal working range. Although the operable read range is confined, the readable range still exists if the AGC is employed. For fixed gain selection, if the gain is set too high, the signal and noise may be amplified to the extent that the following state is unable to discriminate. Using the AGC is optional for users by setting the register **AGCEN** (0x1D.1). If the **AGCEN** is not set, the user can fix the gain of the first two stage amplifier by setting the register **Gain[1:0]** (0x19.[1:0]). The gain of last amplifier, which is not in the AGC loop, can be arbitrarily set to increase total gain from 0 dB to 21 dB through register **Gain_ST3[2:0]** (0x3F.[5:3]). Using this additional gain is recommended for ISO15693 where extended read range is required. In other standards, value of 000b for **Gain_ST3[2:0]** is suggested. Employing this gain state, user shall check that noise from the designed system is not large and does not overwhelm the latter decoder until it is unable to interpret data. **TauAGC** (0x1D.0) is optional for setting the speed of the AGC. If **TauAGC** is set to 0, the time constant of the loop bandwidth equals one period of the operating subcarrier. If **TauAGC** is 1, the time constant equals two periods. In normal condition, setting **TauAGC** to 0 is recommended. If the AGC is not employed, the amplifier gain is defined following Table 6-5.

Table 6-5: Gain of Amplifier of the first two stage in the receiver

Gain[1:0]	Gain
00	12 dB (4x)
01	24 dB (16x)
10	36 dB (64x)
11	48 dB (250x)

In normal operation where the manual-filter-adjustment register **Man_Filter** (0x2F.7) is not set, the filter's frequency corner is automatically defined by the register **SubCarrier[1:0]** (0x19.[4:3]) and **RxCoding[1:0]** (0x1A.[4:3]). The frequency corner is designed by following requirements of the operating standard to cover the power spectrum of the incoming line coding in most situations. Besides, the frequency corner can be arbitrarily adjusted by setting the register **Man_Filter** and specifying desired frequency corner values in the register **Manual filter control** (0x2E). This can be used to cope with distorted bandwidth of the antenna in some circumstances, e.g., detuning of the reader antenna by placing the card very close. In addition, the register **HP2Off** (0x1D.4) and **LP_Off** (0x19.2) are optionally used to deal with the channel bandwidth distortion. Setting **HP2Off** turns off the 2nd-stage high-pass filter in the amplifier chain, resulting in a reduction of spurious collisions due to the residue pulse effect after a large burst of Manchester coding, especially in ISO14443A. Setting **LP_Off** extends the channel bandwidth by trading of increasing of input noise. However, in normal situations, it's recommended to reset both **HP2Off** and **LP_Off**.

6.3.4 Filter tuning system

If the automatic tuning enable register **EnAutoTune** (0x2F.6) is set to 1, the ***Tuning*** command will be activated and the filter tuning system will restore the corner frequencies of the filter to the proper values in order to eliminate results from temperature and process variations due IC manufacturing. Tuning time after activating the command is 302uS. However, the effect from temperature variation is not significant even if the whole IC is heated up by the driver. This process is performed every time the system is powered up. Hence, it is not required to tune the filter frequently by users.

If the **EnAutoTune** is set to 0**,** the corner frequencies of each filter in Figure 6-6 can be manually set by the filter-corner coefficient register **Filter_Corner_Coef** (0x2F.[3:0]). If the **Filter_Corner_Coef** is set to "0000", the corner frequency is set to the highest adjustable value. In contrast, the lowest adjustable corner frequency is obtained when the **Filter_Corner_Coef** is set to "1111".

6.3.5 BPSK-bit decoder

The BPSK decoder converts incoming BPSK streams into digital data bits which are able to be processed by the frame decoder. Register **TauD[1:0]** (0x1D.[4:3]) defines a time constant of the digital phase lock loop (DPLL) used to recover the subcarrier clock from the BPSK line coding. The higher value of **TauD[1:0]**, the longer the locking time but the more stability. However, depending on the preamble length of each standard, users should properly select **TauD[1:0]**. Table 6-6 shows the number of pulses that the DPLL can lock in worst case scenarios. The BPSK stream can be either from the internal data slicer or the external digitized BPSK signal via pin **`SIGIN[1]`**, setting by the register **DecoderSource** (0x1E.0).

Table 6-6: The number of pulse that the DPLL can lock in worst case

TauD[1:0]	The number of pulse can lock
00	10
01	22
10	44
11	88

Furthermore, BPSK decoder for ISO14443A and ISO14443B employs repetitiveness in the data stream of each bit. The decoding method, controlled by **BPSKDecMeth** bit (1Fh.7), can be selected to be either adaptive framing or digital correlator. Both methods can handle BPSK in noisy situation. The adaptive framing is suitable for distorted bit length (ETU) or high jitter base band swinging around normal bit grid. This method can handle consecutive shrunk or extended bit length. The maximum boundary of deviation is +/- 1/8 ETU. The digital correlator is suitable for high jitter base band signal where bit boundary must swing around normal bit grid. This method monitors repetitiveness of data stream to evaluate in coming bit whether it is 1 or 0. The **MinLevel** can set threshold defining validity of incoming bit. For general case, digital correlator is recommended.

6.3.6 Manchester-and-FSK bit decoder

The Manchester-and-FSK bit decoder is capable of decoding both 1-subcarrier Manchester in ISO14443A and ISO15693, and 2-subcarrier Manchester coding (FSK) in ISO15693. The decoder is an analog circuit based on a correlator to search if any incoming signal matches the predefined pattern. The correlator can increase the signal-to-noise ratio, especially, for low data rate in ISO15693 in which the redundancies from long bit patterns are plentiful. Figure 6-7 shows the Manchester-and-FSK bit decoder output from the analog baseband. Each bit interval is divided into half to evaluate output values, collision, and validity, and then deliver to the frame decoder. The triangle shape of the signals in Figure 6-7 are the integrating results of each half bit for evaluation. Each decoded data bit is proven valid if the signal in each half bit is stronger than **Minlevel** threshold, set by the register **Minlevel[2:0]** (0x1D.[3:1]) as shown in Figure 6-7. The lower value of the **Minlevel** results in the higher receiving sensitivity by trading off the receiving errors due to noise. Each decoded data bit is treated to be collided if the signal in the weaker half-bit is relatively larger than the stronger half-bit. The register **Collevel[2:0]** (0x1C.[7:5]) defines such relative level from the stronger half bit.

The **Collevel** value should be set to a proper level for a specific operating mode. If **Collevel** is set too high, the high threshold can cause the codec fail to detect collision due to variations in evaluation resulting from noise or bitphase misaligment. Also, if **Collevel** is set too low, the lower threshold can cause false collisions due to noise or bitphase misalignment. In general transactions where anti-collision is not required, the **Collevel** value should be set to the highest value to prevent errors from collision report due to noise in the system. Effect from **Minlevel** and **Collevel** setting is also illustrated in Figure 6-7. From experiment, the recommended values of **Minlevel** and **Colllevel** setting are shown in Table 6-7.

SubCarrier[1:0], **SubPulse[1:0]** and **RxCoding[1:0]** must be predefined to form expected bit patterns and evaluating intervals. As shown in **Error! Reference source not found.**, the correlator starts operation by relying on the a ctivation of the internal signal ***Start_of_Rx***. Timing of ***Start_of_Rx*** can be controlled by Registers **Rxwait** (0x21) and **Bitphase** (0x1B) where their details will be described in 6.3.8. For low data rate of 6.67kbps and 13.3kbps in ISO15693, setting special control bit **Cont_Int** (0x1E.7) can further increase the gain of the correlator by 4 times and 2 times respectively. This also increases the signal-to-noise ratio by 6 dB and 3 dB accordingly.

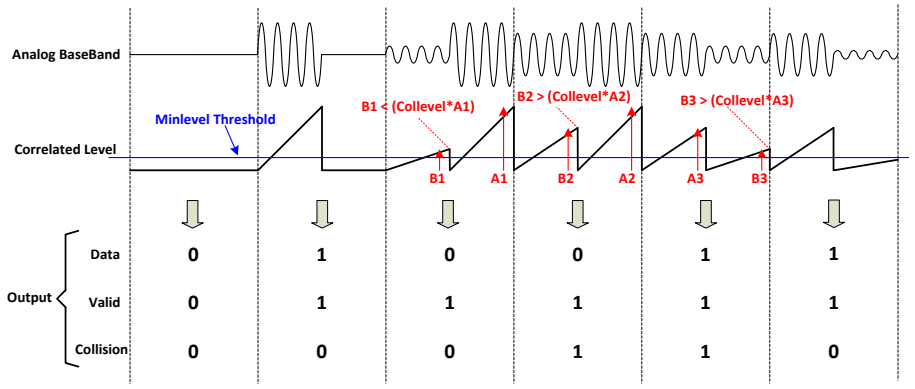


Figure 6-7: Manchester-and-FSK bit decoder output (ISO14443A)

Table 6-7: Typical Value for **Minlevel** and **Collevel**

Standard / Coding	Minlevel[2:0]	Collevel[2:0]
ISO14443A / Manchester (No Anti-Collision)	111b	111b
ISO14443A / Manchester (Anti-Collision)	100b	110b
ISO15693 / Manchester	101b	101b
ISO15693 / FSK	101b	101b

6.3.7 Frame decoder

Depending on operating standards defined by registers **RxFraming** (0x1A.[4:3]) and **SubCarrier**, the frame decoder extracts byte data, checks CRC, parity, and frame formats. Moreover, it removes headers and trailers. Then, the decoded data is transferred to the FIFO.

For Manchester decoding in ISO14443A and ISO15693, if there is a collision of data, the frame decoder detects and reports the first collision of the bit stream in the register **CollPoss** (0x0B). Two optional control registers are provided, namely **CollMarkVal** (0x1A.6) and **ZeroAftercoll** (0x1A.5), to ease the software in manipulating the collision bit in ISO14443A and ISO15693. The collided bits are set to the value following the register **CollMarkVal**. If **ZeroAftercoll** is set, the receiving bit after collision is set to zero.

For BPSK decoding in the ISO14443A, end frame is defined by even parity. For BPSK decoding applied for ISO14443B, registers **NoRxSOF, NoRxEOF** and **NoRxEGT** (0x1D.[7:5]) can be optionally selected to suppress errors due to unusual frame formats that may arise from some cards.

If errors occur during reception, error flags related to decoders, namely **CRCErr**, **FramingErr**, **ParityErr** and **CollErr** (0x0A.[3:0]) are reported.

6.3.8 Timing control generator

The timing control generator provides control signal ***Start_of_Rx*** to start decoding for all types of decoders in the receiver part. Time between the end of the last transmission bit and ***Start_of_Rx*** active, named Twait, is defined by registers **Rxwait** (0x21) and **Bitphase** (0x1B) according to the following relation

$$\text{Twait (Clk)} = \textbf{Rxwait}*\text{ETU} + \textbf{Bitphase}*\text{N}$$

ETU is an elementary time unit of the bit defined by the number of carriers in **SubCarrier[1:0]** and the number of pulses in **SubCpulse[2:0]** as shown in Table 6-8**.** The numbers in yellow boxes are practical numbers for existing modes in supported standards. Table 6-9 shows **SubCarrier[1:0]** and **SubCpulse[2:0]** required for each supported standard. **Bitphase** defined an additional time delay in a fraction of ETU. N, depending on **SubCpulse[1:0]**, is a scaling factor in multiple of clocks as shown in Table 6-10. The Twait is conceptually illustrated in Figure 6-9. The Twait must be properly set to indicate the Manchester-and-FSK bit decoder to start synchronizing with the beginning point of the uplink signal, especially, in ISO14443A at the rate of 106 kbps and ISO15693. In case of BPSK decoding, ***Start_of_Rx*** must be set to active prior to the coming of the uplink signal. Proper values for **Rxwait** and **Bitphase** in each standard are shown in Table 6-11. In addition, if the control signal **RxAutoPD** (0x1E.6) is set, the receiver part is only turned on after the end of the transmission and turned off after the completion of the reception to reduce power consumption of the analog part.

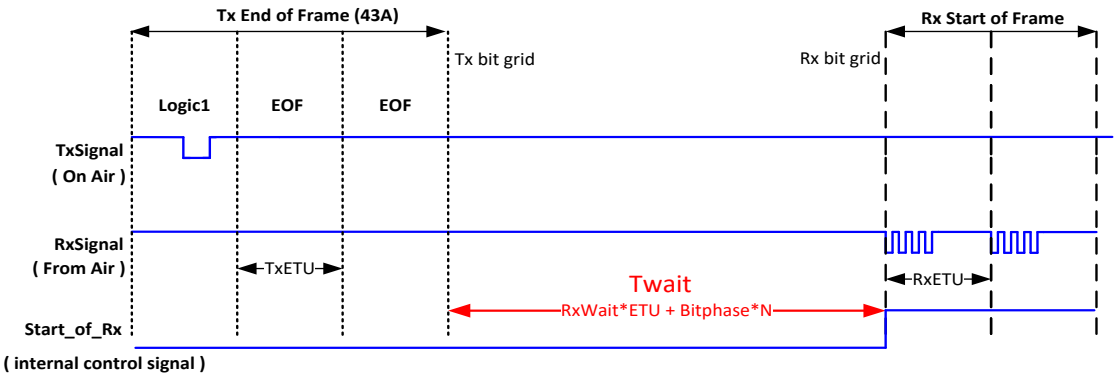


Figure 6-8 Twait**,** timing between TxEOF and RxSOF in ISO14443A at 106kbps

Table 6-8: ETU Interval (in Number of Clocks)

SubCarrier	SubCpulse [2:0]						
	000	001	010	011	100	101	110
	1 Pulse	2 Pulses	4 Pulses	8 Pulse	16 Pulse	32 Pulse	64 Pulse
01 (16 clks)	16	32	64	128	256	512	1024
10 (32 clks)	32	64	128	256	512	1024	2048
11 (64 clks)	64	128	256	512	1024	2048	4096

Table 6-9: Setting of SubCarrier[1:0] and SubCpulse [2:0] for supported standards

SubCarrier [1:0]	SubCpulse [2:0]						
	000	001	010	011	100	101	110
	1 Pulse	2 Pulses	4 Pulses	8 Pulse	16 Pulse	32 Pulse	64 Pulse
01 (16 clks)	14443A/B (848kbps)	14443A/B (424kbps)	14443A/B (212kbps)	14443A/B (106kbps)			
10 (32 clks)				15693 (53kbps)	15693 (26kbps)	15693 (13kbps)	15693 (6.7kbps)

Table 6-10: Scaling factor (N) in multiple of clocks

SubCpulse [2:0]		N
Code	**Number of Pulse**	
000	1 Pulse	1
001	2 Pulses	1
010	4 Pulses	1
011	8 Pulses	1
100	16 Pulses	2
101	32 Pulses	4
110	64 Pulses	8

Table 6-11: Recommended values for Rxwait and Bitphase in each standard

Standard	Downlink	Uplink	RxWait	BitPhase
ISO14443A	Miller – 106kbps	Manch – 106kbps	0x07	0x3D
	Miller – 212kbps	Manch – 106kbps	0x03*	0x88*
	Miller – 424kbps	Manch – 106kbps	0x03*	0x32*
	Miller – 848kbps	Manch – 106kbps	0x03*	0x40*
	Miller -212, 424, 848	BPSK - 212, 424, 848	0x03*	Don't care
ISO14443B	NRZ -106, 212, 424, 848	BPSK - 106, 212, 424, 848	0x03	Don't care
ISO15693	1of4 - 26k, 1of256 - 26k	Manch - 26kbps	0x08	0x40
		Manch - 6.67kbps	0x02	0x0E
		FSK - 26kbps	0x08	0x40
		FSK - 6.67kbps	0x02	0x0E

* The provided values are mean values that can be used for most cards. However, there are different in response timing among various card manufacturers. To achieve highest performance in a certain system or for a specific card, **Rxwait** and **Bitphase** shall be tuned to properly align with the card response.

6.3.9 Key Register Settings for Reception

Table 6-12 shows **RxFraming[1:0]**, **RxCoding[1:0]**, **SubCarrier[1:0],** and **SubCpulse[2:0]** settings for ISO14443A, ISO14443B, and ISO15693.

Table 6-12: xFraming, RxCoding, SubCarrier and SubCpulse settings for supported standards

Standard	Rx Rate	RxFraming[1:0]	RxCoding[1:0]	SubCarrier[1:0]	SubCpulse[2:0]
ISO14443A	Manch 106 kbps	01	00	01	011
	BPSK 212 kbps		01		010
	BPSK 424 kbps				001
	BPSK 848 kbps				000
ISO14443B	BPSK 106 kbps	11	01	01	011
	BPSK 212 kbps				010
	BPSK 424 kbps				001
	BPSK 848 kbps				000
ISO15693	Manch 53 kbps	10	00	10	011
	Manch 26 kbps				100
	Manch 13 kbps				101
	Manch 6.7 kbps				110
	FSK 26 kbps		10		100
	FSK 13 kbps				101
	FSK 6.7 kbps				110

6.4 FIFO Buffer

The RE31 contains a 64-byte FIFO for buffering input and output data stream between the external microcontroller and the internal codec. In normal transmission and reception to/from air, transmitted data should be written into the FIFO before executing. In contrast, reading received data from FIFO can be performed immediately after a single byte of data becomes available. Functions of registers associated with the FIFO are listed in

Table 6-13.

Writing to or reading from the FIFO can be performed through the register **FIFOData** (0x02), while the amount of data remaining in the FIFO is shown by the register **FIFOLength** (0x04). Handling data streams with lengths more than 64 bytes is possible by monitoring the status of flags **LoAlert** (0x03.0) and **HiAlert** (0x03.1), or employing interrupt from **LoAlertIRq** (0x07.0) or **HiAlertIRq** (0x07.0). The **LoAlert** and **HiAlert** are warning flags indicating the amount of data in the FIFO has gone beyond boundary defined by **WaterLevel** (0x21).

The warning flag **HiAlert** is set to 1 by the following equation:

$$\textbf{FIFOLength} \geq (64 - \textbf{WaterLevel})$$

The warning flag **LoAlert** is set to 1 by the following equation:

$$\textbf{FIFOLength} \leq \textbf{WaterLevel}$$

FlushFIFO is a write-only register for content clearance, and resetting the **FIFOlength** and FIFO-overflow flag **FIFOOvf** to zero. To properly access the FIFO, the external microcontroller has to know commands being executed and current states of the internal codec. When the internal state machine of the RE31 grasps either the input end or the output end of the FIFO, accessing such end is prohibited because the higher priority of the internal state machine prevents violated access/interrupt to an executing command. For example, when RE31 is in the receiving state, the FIFO is being written by the internal, the microcontroller cannot write data to the FIFO. By doing so, such reading or writing to the FIFO will not be successful and wrong data may return. Table 6-14 gives an overview of FIFO accessing during command processing.

Table 6-13: Registers associated with FIFO

Register	Address	Indication	Set By	Clear By
FIFOData	0x02	Input end and Output end of buffer for external microcontroller	-	-
FIFOLength	0x04	Number of bytes already stored in the FIFO-buffer (distance between write- and read-pointer)	Write data to FIFO Read data from FIFO	Set **FlushFIFO**
HiAlert	0x03.1	Flag to indicate amount of data in FIFO > (64 - WaterLevel)	FIFO ≥ (64 -WaterLevel)	FIFO < (64 - WaterLevel)
LoAlert	0x03.0	Flag to indicate amount of data in FIFO < WaterLevel	FIFO ≤ WaterLevel	FIFO > WaterLevel
HiAlertIEN	0x06.1	HiAlert interrupt enable	External Controller	External Controller
LoAlertIEN	0x06.0	LoAlert interrupt enable	External Controller	External Controller
HiAlertIRq	0x07.1	HiAlert interrupt flag	**HiAlert** changes from 0 to 1	External Controller
LoAlertIRq	0x07.0	LoAlert interrupt flag	**LoAlert** changes from 0 to 1	External Controller
FIFOOvf	0x09.4	Flag to indicate FIFO was written while FIFO is already full.	Write FIFO while FIFOLength = 64	Set **FlushFIFO**
FlushFIFO	0x09.0	Clear FIFO. FIFOlength becomes zero.	External Controller	-
WaterLevel	0x21	Define the level of FIFO for overflow and underflow warning	External Controller	-

Table 6-14: FIFO Accessible during command processing

Command	Writing FIFO	Reading FIFO	Comment
Idle	OK	OK	Microcontroller can freely access the FIFO.
Transmit	OK	-	Appending data to the FIFO to transmit to air is possible as long as the codec is still in the transmission state.
Transceive	OK	OK	Microcontroller must know the operation state for accessing. Writable the FIFO is allowed in transmitting state. Reading the FIFO is allowed in receiving state. (More information in ***Transmit*** and ***Receive***)
Receive	-	OK	Reading data from the FIFO as soon as data available is recommended to provide ample space of the FIFO especially in case of large amount of data transfer. However, the **FIFOLength** must be monitored to not interpret data from reading when the FIFO is empty (**FIFOLength=0**).
Read EEPROM	-	OK	
Write EEPROM	OK	-	Appending data to the FIFO to use in execution is possible as long as the command is in operating state.
Load Config E2	OK	-	
Calculate CRC	OK	-	
LoadKeyEEPROM	OK	-	
LoadKeyFIFO	OK	-	
Authent	OK	-	
Tune Filter	OK	OK	Microcontroller can freely access the FIFO. No effect to the FIFO from executing this command

6.5 EEPROM

The RE31 contains 256-byte non-volatile EEPROM memory for storing the reloadable user-defined register values, keys for encryption, user data, device ID, and manufacturer information. The EEPROM is organized in 64 blocks of 4 bytes each. Summarized in Table 6-15, accessibility of EEPROM is categorized in three groups: Read Only, Read/ Write and Write Only.

Table 6-15: Accessibility of EEPROM categorized by group

Bytes Address	Block Address	Access Type	Content	Executable Command
0x00 … 0x0F	0x00 … 0x03	Read Only (Write-Protected)	Manufacturer information Manufacturer configuration	***Read EEPROM***
0x10 … 0x6F	0x04 … 0x1C	Read/ Write	User Data Register Initialization	***Read EEPROM*** ***Write EEPROM*** ***Load Config E2*** ***LoadKeyEEPROM*** ***LoadKeyFIFO***
0x70 … 0xFF	0x1D … 0x3F	Write Only (Read-Protected)	Keys for Authentication	***Write EEPROM*** ***LoadKeyEEPROM*** ***LoadKeyFIFO***

The Read-Only addresses (0x00 to 0x0F) are reserved for manufacturer information and configuration; users cannot write data into this area. The content and organization in Read-Only section is shown in Table 6-16.

Table 6-16: Accessibility of EEPROM categorized by group

Address	Block Address	Content Name	Content (MSB … LSB)			
0x0F … 0x0C	0x03	Default Parameter for Analog Part	**Preset Parameters for Analog Part**			
0x0B … 0x08	0x02	Manufacturing information	**R-Txn Conductance**	**R-Txp Conductance**	**Silicon Revision**	**Reserve (00)**
0x07 … 0x04	0x01	RFU	**00**	**00**	**00**	**00**
0x03 … 0x00	0x00	Device Unique ID	**UID**			

The Read/Write addresses can be used to store either reloadable user-defined register values or regular read/write user memory. Contents in the EEPROM can be transferred to set register page by executing a command ***LoadConfig***. This Read/Write area is designed to keep contents of registers up to three sets.

The Write-Only addresses are provided for Crypto_M key storage, and designed to be able to keep keys up to 12 sets. The details of storage keys format are described in section 7.10.1. Executing the EEPROM outside the area that commands can perform stated in Table 6-15 will set bit **AccessError** in the register **Error**. For example, reading from address 0x90 or writing to address 0x00 can cause the bit **AccessError** set.

EEPROM programming time is directly proportional to the number of blocks covering the starting to ending addresses. The programming time of one block takes 4.9 ms. For example, programming from address 0x13 to 0x18 takes triple time of a single block programming, because the programmed addresses span over 3 blocks. The registers associated with the EEPROM are summarized in Table 6-17.

Table 6-17: Registers associated with the EEPROM

Register	Address	Indication	Type	Default Value
Command	0x01	For Activating Write	Read/Write	0
E2Ready	0x05.6	Indicate that EEPROM is ready to program and read.	Read Only	1
TxIRq	0x07.4	Indicate end of EEPROM programming process.	Read/Write	0
E2Err	0x0A	Indicate unsuccessful in EEPROM programming	Write Only	0

6.6 Timer unit

The RE31 contains a timer unit where various events from the RF signal can trigger to start and stop. This feature aids the external microcontroller in monitoring RF events, and enables interrupt-oriented programming. Especially in case of no response from air, interrupt from timer can indicate absence of the incoming signal within a given time. Conceptual diagram of the timer system is depicted in Figure 6-9.

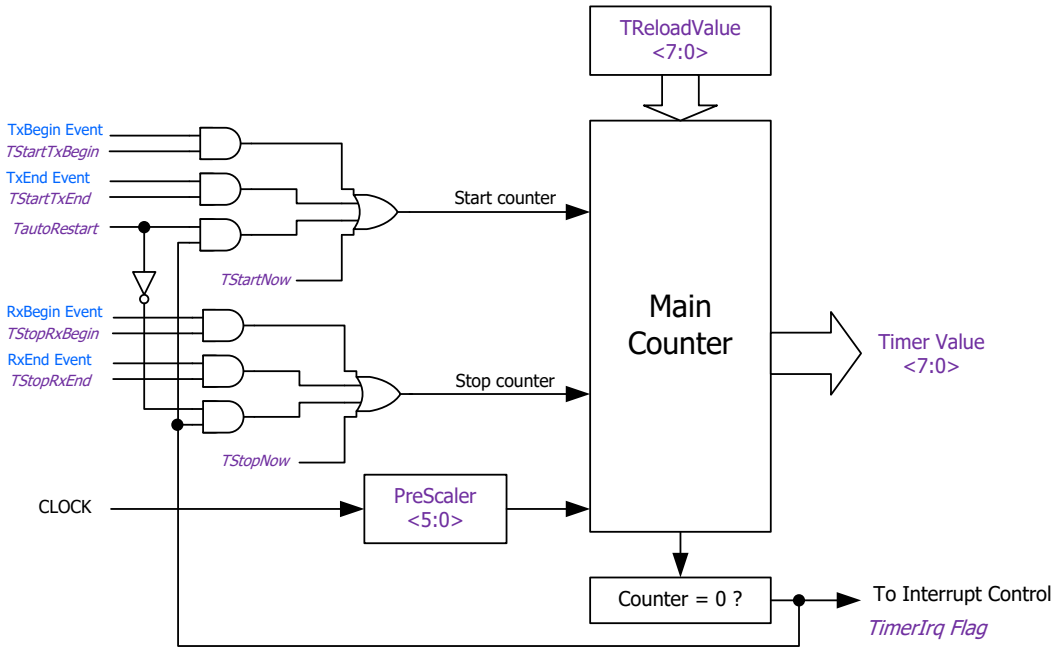


Figure 6-9: Timer Block Diagram

The timer system consists of a main counter, a clock prescaler, a zero-capturing comparator, and an RF event trigger control. The main counter is an 8-bit count-down counter and decreases at the rate of the pre-scaled clock. When the counter is started from defined events, the **TReloadValue** (0x2C) is initialized to the counter. The timer is stopped when the counter value is equal to zero or defined-stop event occurs. Once the timer counter value becomes zero, the timer interrupt flag **TimerIRq** (0x07.5) is set. If **TAutoRestart** (0x2A.5) is set, the **TReloadValue** is reloaded into the main counter when the value in the main counter reaches 1. Then, this will generate interrupt request periodically. However, changing value in the **TReloadValue** during counting will not immediately affect the counter in the current round but it will exhibit in the next start of the trigger. One tick period for updating the main counter is controlled by the prescaler register **TPrescaler** (0x2A.[4:0]), and defined as shown in the relation below

$$\textbf{TPeriod} = (2^{\textbf{TPrescaler}})/13.56\ \text{MHz}.$$

The **TPrescaler** can range from 0 to 21. The external microcontroller can read the current value of the timer from the register **Timervalue** (0x0C). As show in Figure 6-10, the timer value transferring via SPI is latched in the eighth SPI clock after the address is recognized. So, the timer value perceived by the microcontroller lags from the actual value by the period of SPI data transfer.

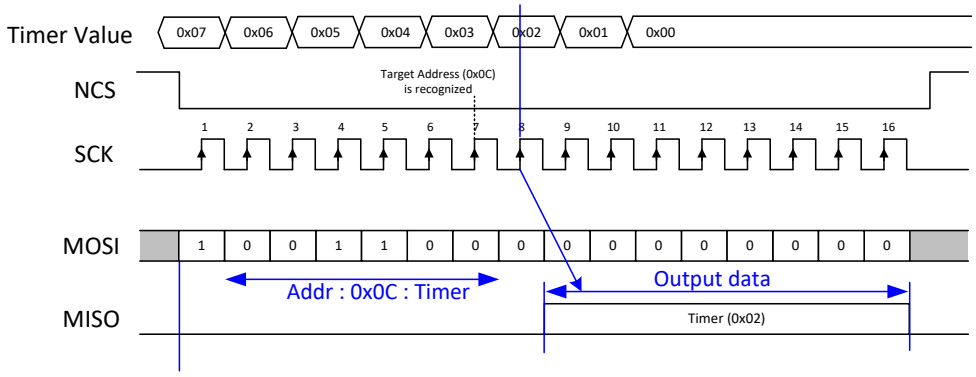


Figure 6-10: Point timer value is latched

The timer can be controlled by events listed below.

- Manually start through setting the register **TstartNow** (0x09.1).
- Manually stop through setting the register **TstopNow** (0x09.2).
- Automatically start when
  - Transmission-beginning event occurs and the register **TStartTxBegin** (0x2B.0) is set.
  - Transmission-end event occurs and the register **TStartTxEnd** (0x2B.1) is set.
- Automatically stop when
  - Reception-beginning event occurs and the register **TStoptRxBegin** (0x2B.2) is set.
  - Reception-end event occurs and the register **TStopRxEnd** (0x2B.3) is set.

The definitions of ending and beginning in the transmission and reception are described in Table 6-18.

Table 6-18: Definitions of ending and beginning in the transmission and reception

Event	Definition
Transmission-beginning	Start of frame of downlink telegram begins to be transmitted
Transmission-end	End of frame or last bit of downlink telegram is transmitted
Reception-beginning	1st valid bit from uplink is received
Reception-end	End of frame of uplink telegram is received or Error occurs during receiving.

Apart from using a time-out feature for no-card-response indicator, the timer can be used for programmable one-shot or periodic trigger. The registers associated with the timer are summarized in Table 6-19.

Table 6-19: Registers associated with the timer

Register	Address	Indication	Type	Default Value
Trunning	0x05.7	The timer is operating	Read Only	0
TimeIEN	0x06.5	The timer interrupt enable	Read/Write	0
TimerIRq	0x07.5	The timer interrupt request occurring if the timer value reaches 0	Read/Write	0
TStopNow	0x09.3	Stop the timer immediately	Write Only	-
TStartNow	0x09.2	Start the timer immediately	Write Only	-
TimerValue	0x0C	Display the current timer value	Read Only	0xFF
TAutoRestart	0x2A.6	Configure the timer to restart automatically after the counter reaches zero. The timer restarts from TReloadValue	Read/Write	0
TPreScaler	0x2A.[5:0]	Clock Prescaler for timer clock	Read/Write	00111
TStopRxEnd	0x2B.3	Set to stop the timer automatically after Rx EOF is found.	Read/Write	0
TStopRxBegin	0x2B.2	Set to stop the timer automatically after Rx SOF is found.	Read/Write	0
TStartTxEnd	0x2B.1	Set to start the timer automatically after Tx EOF is transmitted	Read/Write	0
TStartTxBegin	0x2B.0	Set to stop the timer automatically after Tx SOF is transmitted.	Read/Write	0
TReloadValue	0x2C	Set the timer start values	Read Write	0x0A

6.7 Power Management

The RE31 offers schemes in reducing power during the idle state, namely hard power down, soft power down, Stand by, and Receiver power down modes.

6.7.1 Hard Power Down Mode

If the pin **RSTPD** is set to high, the RE31 goes into the hard power down mode. In this mode, all internal circuits are turned off. The input pin is disconnected from all input pins excluding the pin **RSTPD** itself. Also, accessing to FIFO and registers from the external microcontroller is inhibited. After releasing **RSTPD** to low, the RE31 goes into initializing phase. The external microcontroller can start operating the RE31 when the value in the register command changes from ***Startup*** to idle.

6.7.2 Soft Power Down Mode

The soft power down mode is enabled by setting the bit **PowerDown** (0x09.4) in the **Control** register. In this mode, all internal circuits are turned off but the input and output pins still remain their functionalities. After the **PowerDown** is cleared by the external microcontroller, it takes 1024 clocks, counting from the internal circuit that can detect the first clock signal, for the clock stable period before leaving this mode. The RE31 will completely leave the soft power down mode, if **PowerDown**, where the external microcontroller can monitor, resets itself to zero. If the internal oscillator is used, the time for the oscillator to start-up including clock stable period is typically around 2 ms. Accessing neither FIFO nor registers is allowed except the **Control** register during this power mode.

6.7.3 Stand By Mode

The Stand-by mode is enabled when the bit **Standby** (0x09.5) in the register **Control** is set. In this mode, all internal circuits except the internal oscillator are turned off. After clearing **Standby** by the microcontroller, it takes 4 clocks to leave this mode. Hence, this mode is suitable for applications required fast wake-up. The input and output pins still remain their functionalities as same as that of the soft power down mode.

6.7.4 Receiver Power Down Mode

The receiver power down mode is a power saving mode that turns the receiver circuit off when it is not required for operations, such as in Transmit state or Idle state. By setting the bit **RxAutoPD** (0x1E.6) in **RxControl2** register, the receiver is only active in the states RxPrepare and Receiving. If this bit is cleared, the receiver circuit is always turned on. It is recommended to enable this mode.

6.8 Interrupt system

The RE31 is comprised of six sources of interrupts available to serve interrupt-oriented programming. The interrupts indicates key events related to RE31 peripherals, i.e., CODEC, FIFO, EEPROM, and timer. When the interrupt requests occur, they are reported in three ways: a register **InterruptFlag** (0x07), a bit **IRQ** (0x03.3) in **PrimaryStatus** register, and a signal level on pin **IRQ**. If one of **InterruptFlag** is set while its corresponding **InterruptEnable** bit (0x06.x) is also set, the register bit **IRQ** is set and the pin **IRQ** toggles to its active state. Polarity of the pin **IRQ** can be suitably set either active high or low for the microcontroller by the register **IRQInv** (0x31.0). Table 6-20 summarizes indications of the interrupt flags, and suggests next actions for the microcontroller. To set or clear **InterruptFlag** or **InterruptEnable**, the external microcontroller can perform through writing the target interrupt bit with writing-control bits **SetIEN** or **SetIRq** in (0x06.7 or 0x07.7) respectively. If **SetIEN** or **SetIRq** is written by value 1, the set bits in **InterruptEnable** or **InterruptFlag** are set. The unset bit in such register remains unchanged. Also, if **SetIEN** or **SetIRq** is written by value 0, the set bits in **InterruptEnable** or **InterruptFlag** are cleared. Multiple bits of **Interrupt Flag** or **Interrupt Enable** can be written concurrently. For example, writing 0x3F to the **InterruptEnable** clears all interrupt enable bits. Writing 0xBF to the **InterruptEnable** sets all interrupt enable bits. The **InterruptFlag** is usually set by the internal state machine and cleared by the external microcontroller, while **InterruptEnable** is always set and cleared by the external microcontroller.

Table 6-20: Source of interrupt triggering and suggested action for microcontroller

Interrupt Flag	Indication when interrupt is set	Suggested action for microcontroller
TimerIRq	Timer decreases from 1 to 0 or set-up time is up.	Investigate cause of time out
TxIRq	One of these events in these commands occurs : - ***Transmit*** : All data transmitted. - ***Transceive*** : All data transmitted.	Start Receive command or start other command.
	One of these events in these commands occurs : - ***Tuning*** : Tuning process finishes. - ***WriteE2*** : All data is programmed. - ***CalCRC*** : All data is processed.	Begin to start other command.
	One of these events in these commands occurs : - ***LoadKeyEEPROM*** : Key is already in buffer - ***LoadKeyFIFO*** : Key is already in buffer	Start Authentication command.
RxIRq	Receiver finishes reception in both cases of successful and error.	Read Data from the FIFO. Investigate received data and process for the next transmission.
IdleIRq	Operation of command is finished and state is changed to idle. End of operation of all commands causes **IdleIRq** set to 1. Setting power down or standby during executing or starting ***Idle*** command does not set **IdleIRq**.	Begin to start other command.
HiAlertIRq	The FIFO is getting full and **FIFOlength** > 64 - **Water_Level**.	Read Data from the FIFO to prevent the FIFO Full.
LoAlertIRq	The FIFO is getting empty and **FIFOlength** < **Water_Level**.	Write Data to the FIFO if need.

6.9 Crypto_M engine

The RE31 incorporates a Crypto_M engine to encrypt the transmitted data, and decrypt the received data. A diagram of transmission and reception systems with a crypto engine is shown in Figure 6-11. Before process encrypting and decrypting in read/write operations from/to Crypto_M card, the 48-bit keys of the data section being accessed in the card must be previously loaded to the key buffer and the authentication process must be successful. A block diagram in Figure 6-11 shows inter-block activities for commands associated with key loading. Bit **Crypto_MOn** (0x09.3) indicates the completion of the authentication process. This Crypto engine is only applicable for transactions in ISO14443A at 106 kbps.

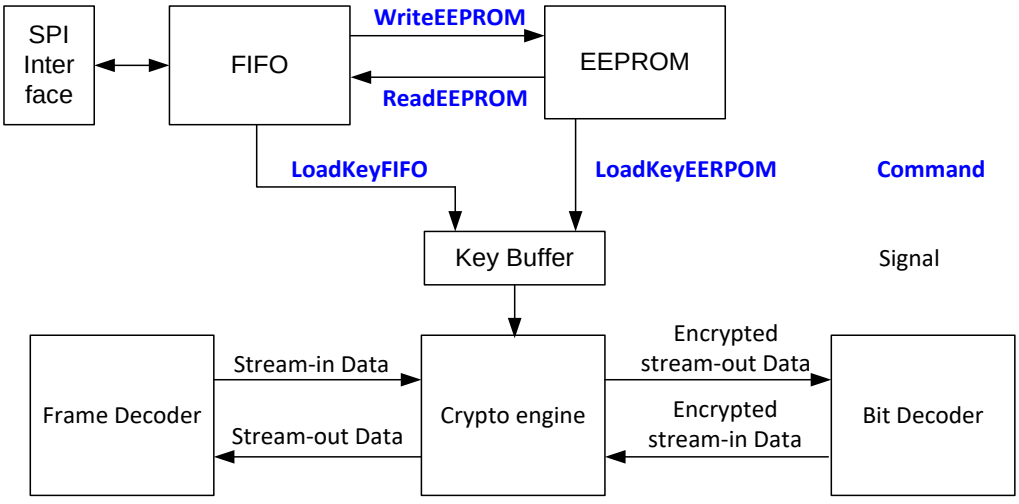


Figure 6-11: Diagram of transmission and reception systems with a crypto engine

6.10 Regulator

The RE31 contains two on-chip 80-mA regulators. Typically, the output voltage is 3.2 Volt. The typical connection is shown in Figure 6-12. A 100-nF ceramic capacitor and a 10-uF tantalum are suggested to connect to the regulator output for stability and supplying high frequency current to a particular section. As shown in Figure 6-12, the first regulator on pin **VREGA**, is used to supply an analog part of the RE31, while the other on pin **VREGO** is used for a digital part and an external microcontroller. In applications where noise is a major concern, for example mid/long-range readers, ferrite beats can be inserted in supply buses as shown in Figure 6-13 to attenuate interference among each other.

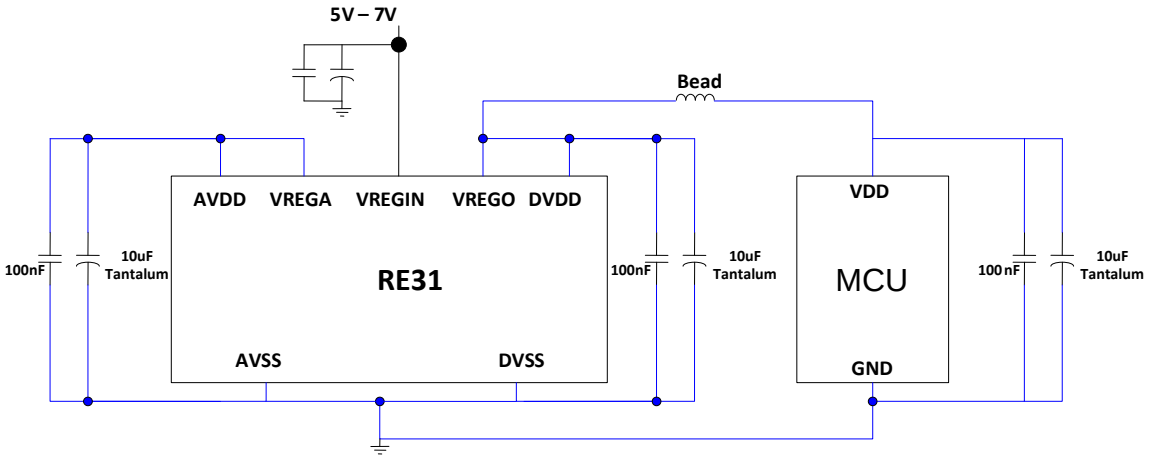


Figure 6-12: Typical power supply connection

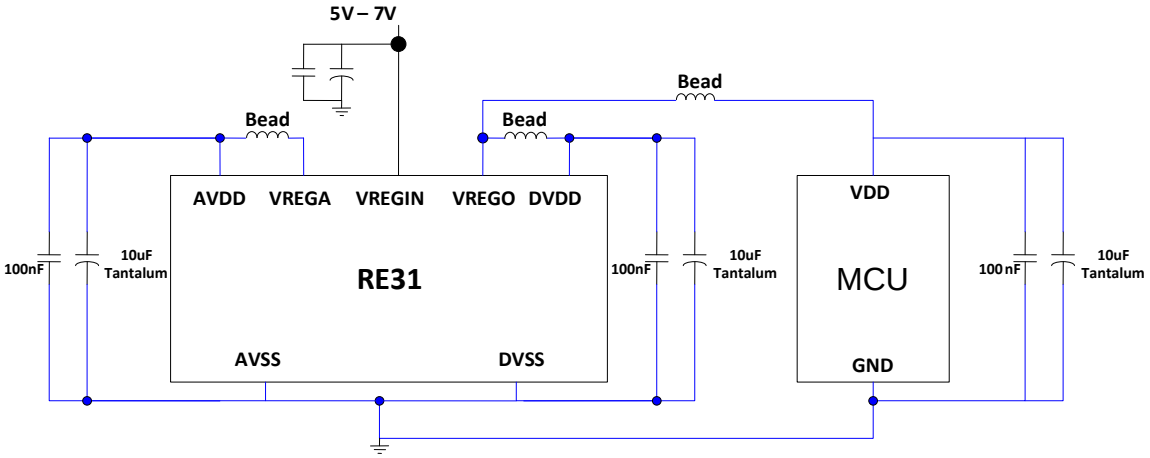


Figure 6-13: Typical power supply connection with ferrite beats used in low noise systems

Figure 3-8 shows regulated characteristics of the regulators. At 80-mA rated load, the on-chip regulators can fully operate when the regulator input voltage at pin **VREGIN** is fed by voltages more than 4.8 volt. Figure 3-6 shows line regulation with increasing input voltage. The line regulation is typically 0.5 mV/V. Figure 3-7shows load regulation. The load regulation is 0.25 mV/mA.

More important points, the regulator also generates additional heat due to drop-in voltage and current pass through. This amount of heat must be taken into account for heat dissipation design.

7. RE31 COMMAND

To perform RF interface or internal activities of the RE31, an external microcontroller has to write a specific command to the **Command** register in address 0x01. Available commands and input/output data associated with the FIFO are summarized in Table 7-1.

Table 7-1: RE31 Command

Command	Code	Action	Input Data Required in FIFO	Return Data Read from FIFO
Startup	0x30	Indicate external microcontroller that the RE31 is in initializing state	-	-
Idle	0x00	Idle or cancel current executing command except write EEPROM Command, LoadKeyEEPROM, LoadKeyFIFO	-	-
Transmit	0x1A	Transmit data in the FIFO buffer to air.	Data stream	
Receive	0x16	Enable receiving circuit and decode signal form air into data in the FIFO.		Data stream
Transceive	0x1E	Transmit Data in the FIFO buffer to card and enable receiving circuit after transmission complete. Then, put the received data into the FIFO.	Data stream	Data stream
WriteEEPROM	0x01	Write data in the FIFO buffer to the EEPROM	Start Address + Data stream	-
ReadEEPROM	0x03	Read data from the EEPROM and store into the FIFO buffer	Start Address + Number of Address	Data stream
CalCRC	0x12	Perform CRC calculation from available data in the FIFO	Data stream	-
LoadConfig	0x07	Read data from the EEPROM to initialize the register page	Start Address	-
LoadKeyEEPROM	0x0B	Read data from the EEPROM and put into the key buffer. Key data in the EEPROM must be in the specific format	Start Address	-
LoadKeyFIFO	0x19	Read data in the FIFO and put into the key buffer. Key data must be in the specific format	Byte0 (LSB) + Byte1+… +Byte10+Byte11	-
Authent	0x0C	Execute authentication to turn crypto engine on.	Tag's Authent command + Tag's Block Number+ Tag's UID(LSB) + … Tag's UID(MSB)	-
TuneFilter	0x10	Execute filter tuning process	-	-

7.1 *Startup* Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x30	Indicate external microcontroller that RE31 is in initializing state	-	-	-

The ***Startup*** command is started by the internal state machine automatically after reset. It is used to indicate the external microcontroller that the RE31 is initializing and the external microcontroller should wait until the command register switches from the ***Startup*** to 0x00 (idle state) before performing any execution. This command is for the internal state machine only; users cannot start this command from the external microcontroller.

7.2 *Idle* Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x00	Idle or cancel executing command except write EEPROM Command, LoadKeyEEPROM	-	-	-

The ***Idle*** command stops the current executing command. Consequently, the current state is set to idle state while non-processing data in the FIFO buffer remains unchanged. Note that the **IdleIrq** flag in the **Interrupt Flag** register is not set by the activation of this command. However, commands ***WriteEEPROM***, ***LoadKeyFIFO*** and ***LoadKey*** are not affected from issuing ***Idle***. These commands still continue to operate to prevent detrimental effects to the IC system i.e. memory damage.

7.3 *Transmit* Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x1A	Transmit Data in FIFO buffer to card	Data stream	-	TxIrq, IdleIrq

The ***Transmit*** command conveys data from the FIFO buffer to the transmitter to modulate carriers. The RF bit pattern of the transmitted data is formed by following the defined protocol, configurable in transmitter-related register page (page 3). Basically, there are two basic schemes in transmitting data on air: *Write-FIFO-before-Transmit* and *Transmit-before-Write-FIFO*. Assume that the current state of the codec is idle; steps and results of both schemes are described below.

Table 7-2: *Transmit* Command : Write FIFO before Transmit

Step		Results
1	Write data to be transmitted to the FIFO.	- Data is in the FIFO.
2	Write ***Transmit*** to **Command** Register.	- Data in the FIFO is transmitted on air until the FIFO is empty. - The **TxIrq** and **IdleIrq** Interrupt flags are set.

The maximum data that can be transferred by this method is 64 byte.

Table 7-3: *Transmit* Command : Transmit before Write FIFO

Step		Results
1	Write ***Transmit*** to **Command** Register.	- The CODEC is in a transmission preparation state.
2	Write data to be transmitted to FIFO.	- The CODEC starts transmission as soon as the first byte is written to the FIFO. - Data in the FIFO is transmitted as long as the FIFO is not empty. - The CODEC stops transmission and appends EOF when the FIFO has reached empty state. - The **TxIrq** and **IdleIrq** Interrupt flags are set.

This method continues transmission as long as the data of the next byte still available in the FIFO. This method allows transmission of the data more than 64 bytes. The microcontroller must put the data stream in the FIFO buffer soon before the FIFO becomes empty. A combination of these two methods, which is writing some data to the FIFO first and appending after transmission, is possible. It does yield an effective transmission for long data stream. If no more data available in the FIFO, the CODEC appends CRC and EOF at the end, and switches to idle state. The state machine leaves the transmission state to idle state, and the **TxIrq** and **IdleIrq** flags are set.

7.3.1 CRC and Parity

The transmission telegram can be composed of CRC and parity bits, by enabling the bit **TxCRCEn** and the bit **ParityEn** in **Channel Redundancy** register. The CRC result is relied on the CRC calculation method in the bit **MSBFirst**, **CRC3309** and preset values in **CRC Preset LSB** and **CRC Preset MSB**. If **TxCRCEn** is set, two CRC bytes are appended following the last byte from the FIFO. Except the bit-oriented transmission and the short frame in ISO14443A, the **TxCRCEn** should be used in all protocols. If the bit **ParityEn** in **Channel Redundancy** register is set, parity bits are inserted between each transmitted byte in the telegram. The polarity of the parity bit is controlled by the **ParityOdd** bit in the **Channel Redundancy** register. The parity bit is only allowed in ISO14443A.

7.3.2 Bit oriented transmission in ISO14443A

For bit-oriented transmission in ISO14443A, the number of bits in the last transmitted byte can be controlled via the register **TxLastBit** in the register **BitFraming**. The **TxLastbit** is a three-bit register; its value reflects the number of bits in the last byte. Only the least significant bit of the last byte following the defined number is transmitted. If **TxLastbit** is set to 0, the whole last byte is transmitted. Figure 7-1 illustrates the example of bit-oriented transmission telegram with effect of **TxLastbit**. The **TxLastbit** is only applicable to the ISO14443A setting and have no effect on other standard settings.

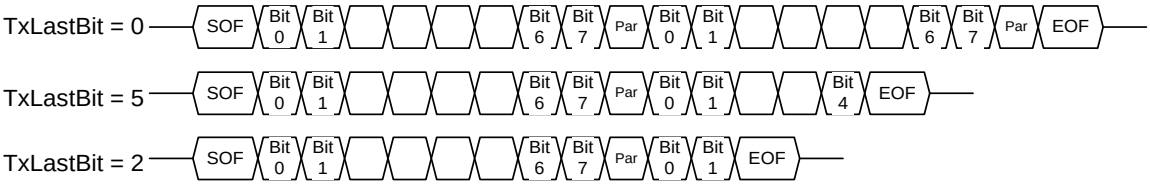


Figure 7-1: Effect of **TxLastbit** in bit-oriented transmission telegram (Assume two bytes in the FIFO)

7.3.3 Transmission timing

In case of transmitting data more than 64 byte, the external microcontroller must input data to the FIFO during transmission before the last bit, where the FIFO Length is zero, is transmitted on-air. To transfer data without interruption, the FIFO level monitoring through low-alert interrupt must be employed. New data written after last-bit transmission is neglected and remains in the FIFO. If **TxLastbit** is not equal to 0, the data for transmission must be available in the FIFO before the indicated last bit is transmitted. Figure 7-2 illustrates the time line that the codec decides to end or continue the transmitting stream.

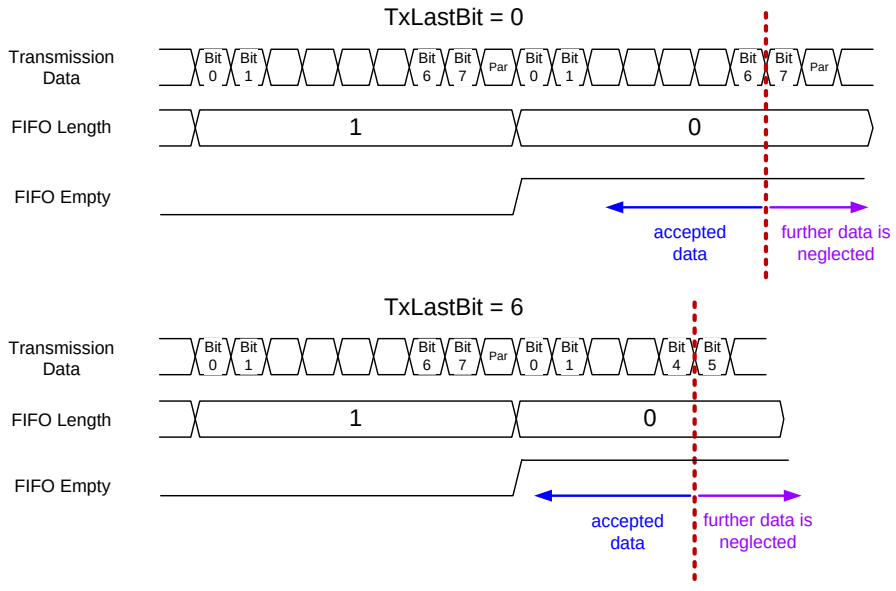


Figure 7-2: Timing for appending data before transmission ends

7.3.4 Sent1Pulse

In ISO15693, there is a requirement to send a single RF gap on air to indicate next slot during anti-collision. Regardless of data in the FIFO, setting bit **Sent1Pulse** (0x14.7) and then writing ***Transmit*** to the **Command** register produces a gap on the RF signal. Note that it is required that **CoderRate** and **TxCoding** must be set in ISO15693 mode.

7.3.5 Register related to transmission

The register related to transmission and transmitter configurations are summarized in this Table 7-4.

Table 7-4: Register related to transmission

Register	Address	Indication/Usage	Type	Default Value
Command	0x01	Activate ***Transmit*** or ***Transceive*** command	Dynamic	0x00
TxIEN	0x06.4	Configure interrupt enable for TxIRq	Read/Write	0
TxIRq	0x07.4	Indicate data was transmitted	Dynamic	0
TxLastBits	0x0F	Define the number of bits in the last transmitted byte.	Dynamic	000
TxControl	0x11	Configure driving behaviour of the transmitter	Read/Write	0x58
GsCfgCW	0x12	Configure output conductance of the transmitter during carrier transmission	Read/Write	0x3F
GsCfgMod	0x13	Configure output conductance of the transmitter during carrier modulation	Read/Write	0x28
Send1Pulse	0x14.7	Configure to sent 1 pulse in ISO15693	Read/Write	0
CoderRate	0x14.[5:3]	Configure transmitter data rate	Read/Write	011
TxCoding	0x14.[2:0]	Configure transmitter coding	Read/Write	001
ModWidth	0x15	Define modulation width of data bit in ISO14443A and ISO 15693	Read/Write	0x0F
ModWidthSOF	0x16	Define modulation width of SOF bit in ISO14443A and ISO 15693	Read/Write	0x0F
NoTxSOF	0x17.7	Suppress SOF transmission in ISO14443B	Read/Write	0
NoTxEOF	0x17.6	Suppress EOF transmission in ISO14443B	Read/Write	0
EOFWidth	0x17.5	Define width of EOF in ISO14443B	Read/Write	1
CharSpacing	0x17.[4:2]	Define the number of EGT in ISO14443B	Read/Write	110
SOFWidth	0x17.[1:0]	Define width of SOF in ISO14443B	Read/Write	11
MSBFirst	0x22.6	Define method in calculation CRC	Read/Write	0
CRC3309	0x22.5	Define method in calculation CRC	Read/Write	0
CRC8	0x22.4	Define method in calculation CRC	Read/Write	0
TxCRCEn	0x22.2	Enable CRC in transmitted frame	Read/Write	0
ParityOdd	0x22.1	Set odd parity in transmitted frame	Read/Write	1
ParityEn	0x22.0	Enable parity in transmitted frame	Read/Write	1
CRCPresetLSB	0x23	Define preset CRC value in LSB	Read/Write	0x63
CRCPresetMSB	0x24	Define preset CRC value in MSB	Read/Write	0x63

7.4 *Receive* Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x16	Enable Receiving circuit	-	Data stream	RxIrq, IdleIrq

The ***Receive*** command starts the receiver circuit and returns decoded data in byte to the FIFO. Also, the ***Receive*** command, starting automatically after the transmission has finished, is the second part of ***Transceive*** command.

After executing the ***Receive*** command from SPI, the CODEC state-machine changes to "***RxPrepare***" state and delays start of the receiver by the number of ETU defined in register **RxWait**. If the ***Receive*** command is automatically issue as of part the ***Transceive*** command, the time delay defined by register **Bitphase** is inserted to adjust Rx-bit grid suitably align for tag response. The timing in Figure 7-3 shows behavior of ***Receive*** command in RE31. Firstly, the receiver is restarted synchronously to the previous running Rx-bit grid, referring from end of last transmission. Then, state changes to "***RxAwaiting***" state and CODEC looks for the data pattern that matches the predefined SOF. Once the SOF is detected, the state machine changes to ***"Receiving"*** state and continues to decode the incoming signal into data byte and store in the FIFO. The state machine leaves ***"Receiving"*** state if no further data is received or an error occurs during receiving. If the bit **RxMultiple** is cleared, the state changes to ***"Idle"*** state and the **RxIrq** and **IdleIrq** are set. On the other hands, if the bit **RxMultiple** is set, only the ***RxIrq*** is set. Then, the state returns to ***"RxPrepare"*** state and delay start of receiver following register **RxWait**, which also synchronize to the previous Rx-Bit grid as shown in Figure 7-4.

For long received data stream more than 64 bytes, the microcontroller must manage FIFO accessing routine to prevent overflow. Therefore, **HiAlert** Interrupt can be employed in monitoring. The state of reception is shown in Figure 7-6. Note that the analog receiver circuitry requires time to initialize and warm-up before decoding signal. It is necessary to set the register RxWait with the minimum value for RxWait of 3.

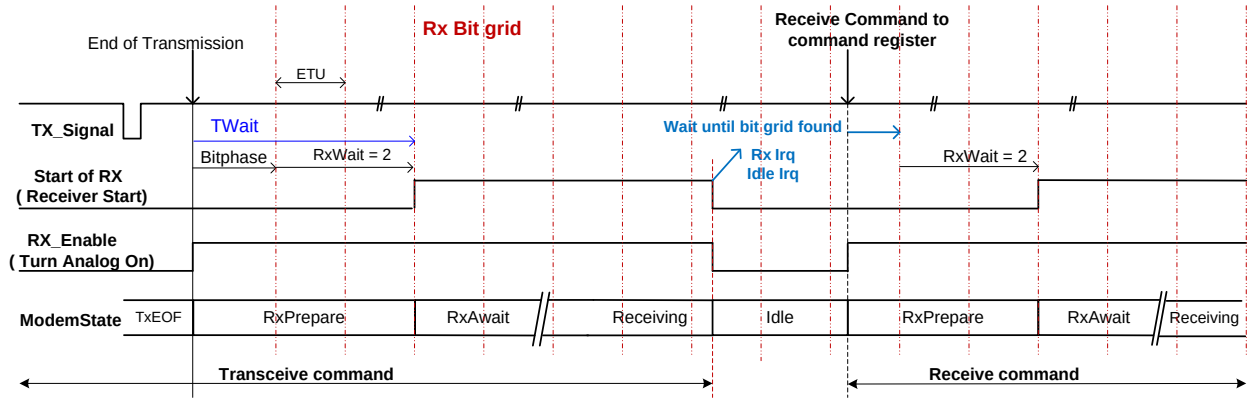


Figure 7-3: Timing of ***Transceive*** and ***Receive*** command

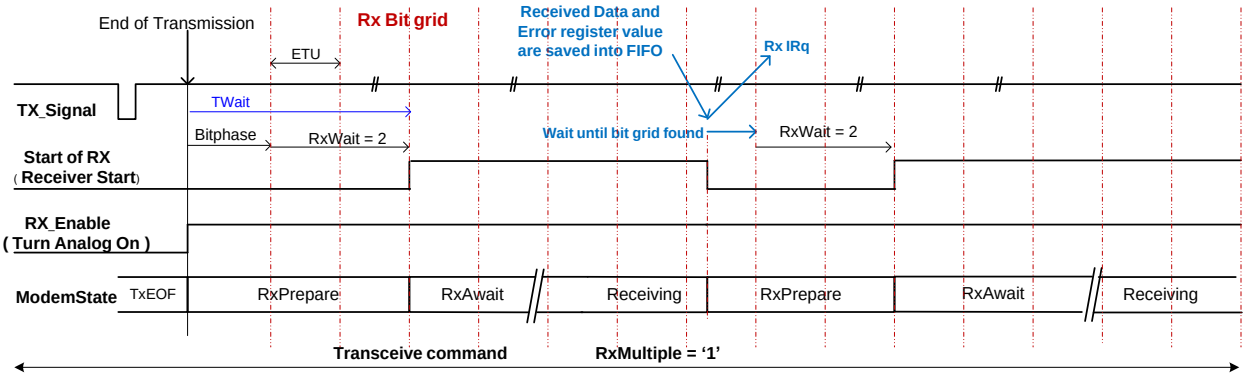


Figure 7-4: Timing of ***Transceive*** command with **RxMultiple** bit is set

7.4.1 CRC and Parity

If the bit **RxCRCEn** in the **Channel Redundancy** register is set to expect CRC in received telegram, the last two bytes of the received frame are treated as a CRC of the preceding data stream. If the received CRC is identical to the calculated CRC from the CODEC, the preceding received data is successful without a CRC error and the CRC is not loaded to the FIFO buffer. The result of CRC is displayed in registers **CRCResultLSB** and **CRCResultMSB**. On the other hand, the received mismatched CRC will be forwarded to the FIFO and the bit **CRCError** in the **Error** register is set.

In case of parity, if the bit **ParityEn** is set in the **Channel Redundancy** register, the parity is expected after the end of each byte. If the received parity is not equal to the expected setting from the bit **ParityOdd** in the **Channel Redundancy** register, the bit **ParError** in the **Error** register is set. The parity checking only performs in ISO14443A standard. The **ParityEn** bit have no effect on reception of other standard settings.

7.4.2 Collision Detection

If more than one card present in the same RF-field, the data collision can be occurred. If there is a collision, the bit **CollError** in the **Error** Register is set and the collision position of the received bit stream is displayed in the collision position register **CollPos**. Figure 7-5 shows examples of **CollPos** values and the meaning of collision bits. As stated in 6.3.7, the collided bits can be set to a value in **CollMarkVal** and the receiving bit after collision can be forced to zero by setting the bit **ZeroAftercoll.** This feature is to ease software in manipulating anti-collision mechanism in ISO14443A at the data rate of 106 kbps and ISO15693 at all rates.

Table 7-5: Example of Collision position and reported value of CollPos

Position	CollPos value	Comment
SOF	0	**FramingErr** is also set
1st bit of 1st byte	1	
2nd bit of 1st byte	2	
8th bit of 1st byte	8	
Parity of 1st byte	8	**ParityErr** is also set
1st bit of 2nd byte	9	
7th bit of 2nd byte	15	
Parity of 2nd byte	16	**ParityErr** is also set

7.4.3 Receiving of bit oriented for ISO14443A

During anti-collision process in ISO14443A, the first received byte may be partially transmitted from the card. For reception of such split byte, **RxAlign** in the **BitFraming** register defines the first received bit position in the first decoded byte. **Error! Reference source not found.**Figure 7-5 shows the evaluated data byte when setting **RxAlign** at different values. Assume that the bit **ParityEn** equals 1. If **RxAlign** is not equal to zero, the parity of the first byte is not checked.

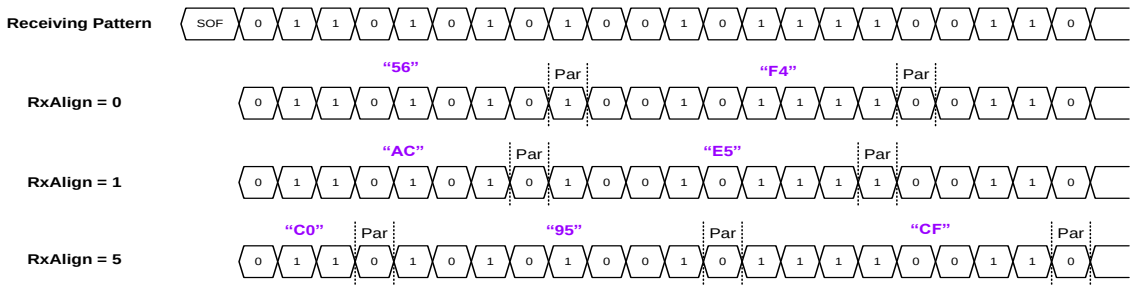


Figure 7-5: Example of evaluated data for different **RxAlign** settings

7.4.4 Error in receiving

At the end of reception, some errors in reception are indicated in **Errorflag** in the **Error** register. The meaning of the error flags related to the reception is described in Table 7-6.

Table 7-6: Error flag related to RF reception

Error Flag	Event
FramingError	Invalid frame format, namely - SOF and EOF don't conform to the standard defined in the receiver. - EGT in ISO14443B is incomplete.
ParityError	Wrong parity received in ISO14443A
CRCError	Wrong CRC received
CollError	Collision detected in ISO14443A and ISO15693

7.4.5 EMD Suppression

Conventionally, to handle frame contain EMD, microcontroller must consider received frame if it is EMD by relying on interrupt signal after end of reception and already-received data in FIFO. Although, the **RxMultiple** bit or ***Receive*** command can assist this operation, such operation takes significant time from transaction between microcontroller and RE31 via SPI. Then, response time is quite long.

The RE31 contains EMD suppression function, which is a feature designed to reduce microcontroller task in handling EMD frame reception. When bit **EMD_Suppress** (0x1F.1) is set, if the number of received data byte is less than 3 bytes and frame contains errors related to reception namely **CRCErr, FramingErr, ParityErr, CollErr**, system automatically discards the received data and returns to ***"RxAwaiting"*** state to receive next frame as shown in Figure 7-6. If the number receiving byte is more than 3 bytes, EMD suppression feature is not function because it is treated as normal data frame which is usually consisted of one data byte and two associated CRC. The EMD suppression is applicable for ISO14443A protocol, ISO14443B protocol, **RxMultiple** setting and ***Receiving*** command. For some reception frame such as ATQA or part of UID in which response is less than 3 bytes and no error, received data will be passed to FIFO. Hence, **RxCRCEn** shall be set correctly for expected response. When any suppression is detected, **EMD_Det** bit (0x05.4) is set.

7.4.6 Register related to reception

The registers related to reception are summarized in this Table 7-7.

Table 7-7: Register related to Reception

Register	Address	Indication/Usage	Type	Default Value
Command	0x01	Activate ***Receive*** or ***Transceive*** command	Dynamic	0x00
RxLastBits	0x05.[2:0]	Displays the number of valid bits in the last received byte	Read Only	000
RxIEN	0x06.3	Configure interrupt enable for RxIRq	Read/Write	0
RxIRq	0x07.3	Indicate end of reception	Dynamic	0
CRCErr	0x0A.3	Report CRC error in received frame	Read Only	0
FramingErr	0x0A.2	Report Framing error in received frame	Read Only	0
ParityErr	0x0A.1	Report Parity error in received frame	Read Only	0
CollErr	0x0A.0	Report data collision in received frame	Read Only	0
CollPos	0x0B	Report collision position in ISO14443A / ISO15693	Read Only	0
RxAlign	0x0F.[6:4]	Define the position of the first received data bit to be stored in the first received byte in the bit oriented frame in ISO14443A	Dynamic	000
SubCpulses	0x19.[7:5]	Define the number of carriers in subcarrier	Read/Write	011
SubCCarrier	0x19.[4:3]	Define the number of carrier clocks used in subcarrier.	Read/Write	01
LP_Off	0x19.2	Switch off all Lowpass filters to extend incoming signal bandwidth.	Read/Write	0
Gain[1:0]	0x19.[1:0]	Define Gain of Amplifier manually	Read/Write	11
RxMultiple	0x1A.7	Set to receive consecutive reception	Read/Write	0
CollMaskVal	0x1A.6	Set to value of collided bit	Read/Write	0
ZeroAfterColl	0x1A.5	Set to value of data collided bit to be zero	Read/Write	0
RxFraming	0x1A.[4:3]	Define decoder framing	Read/Write	01
RxCoding	0x1A.[1:0]	Define receiving pattern for decoder	Read/Write	00
Bitphase	0x1B	Define the fractional guard time	Read/Write	0x60

		decoder in unit of clock.		
MinLevel	0x1C.[7:5]	Define the minimum signal strength at the decoder input that shall be accepted.	Read/Write	011
CollLevel	0x1C.[3:1]	Define the relative minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester and FSK-coded signal.	Read/Write	011
NoRx_SOF	0x1D.7	Suppress error from SOF-missing frame	Read/Write	0
NoRx_EGT	0x1D.6	Suppress error from EGT not confirming the standard	Read/Write	0
NoRx_EOF	0x1D.5	Suppress error from EOF-missing frame	Read/Write	0
HP2Off	0x1D.4	Switch off the 2nd high pass filter	Read/Write	0
TauD	0x1D.[3:2]	Defines time constant of internal PLL.	Read/Write	01
AGC_EN	0x1D.1	Enable Automatic gain control	Read/Write	1
TauAGC	0x1D.0	Define time constant of AGC	Read/Write	0
Cont_Int	0x1E.7	Boost correlator gain by 4X in lowdata rate of ISO15693.	Read/Write	0
VMidSel	0x1E.5	Select Reference for VMID	Read/Write	1
ByPassEnv	0x1E.2	Select type of analog input signal present at Rx pin for extension in long range application	Read/Write	0
DecoderSource	0x1E.0	Select input signal for internal decoder	Read/Write	1
BPSKDecMeth	0x1F.7	Define the BPSK Decoding Method.	Read/Write	1
BPSKDataRec	0x1F.6	Enable BPSK Data Recognition block	Read/Write	1
SOFSel15693	0x1F.5	Define the method of ISO15693 header recognition	Read/Write	1
EMD_Suppress	0x1F.1	Enable EMD frame suppression	Read/Write	0
SOFSel43A	0x1F.0	Define the ISO14443A SOF condition.	Read/Write	0
RxWait	0x21	Define guard time counting from TxEOF to start of receiving time of decoder in unit of one-bit duration	Read/Write	0x06
MSBFirst	0x22.6	Define method in calculation CRC	Read/Write	0
CRC3309	0x22.5	Define method in calculation CRC	Read/Write	0
CRC8	0x22.4	Define method in calculation CRC	Read/Write	0
TxCRCEn	0x22.2	Enable CRC in transmitted frame	Read/Write	0
ParityOdd	0x22.1	Set odd parity in transmitted frame	Read/Write	1
ParityEn	0x22.0	Enable parity in transmitted frame	Read/Write	1
CRCPresetLSB	0x23	Define preset CRC value in LSB	Read/Write	0x63
CRCPresetMSB	0x24	Define preset CRC value in MSB	Read/Write	0x63
M_HP1	0x2E.[7:6]	Define high-pass corner frequency for 1st stage high pass filter	Read/Write	00
M_LP1	0x2E.[5:4]	Define low-pass corner frequency for 1st stage low pass filter	Read/Write	01
M_HP2	0x2E.[3:2]	Define high-pass corner frequency for 2st stage high pass filter	Read/Write	10
M_LP2	0x2E.[1:0]	Define low-pass corner frequency for 2st stage low pass filter	Read/Write	01
Man_Filter	0x2F.7	Define to configure frequency corner of filter manually.	Read/Write	0

7.5 Transceive Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x1E	Transmit Data in the FIFO to card and enable receiving circuit after transmission completed.	Tx Data stream	Rx Data stream	TxIrq, RxIrq, IdleIrq

The ***Transceive*** command starts the ***Transmit*** command first and then automatically executes the ***Receive*** command when the ***Transmit*** is finished. Therefore, the transmitted data must be written to FIFO during transmission process and the received data stream is returned into FIFO during reception. In transceiving data more than 64 bytes, the FIFO handling routines through interrupt indication, such as HiAlert and LoALertsimilar to that of Transmit and Receive, must be employed.

7.5.1 State Machine

The state of CODEC can be monitored via the **ModemState** value in the **PrimaryStatus** register. The state transition diagram including the triggering event, related interrupt flag are shown in Figure 7-6.

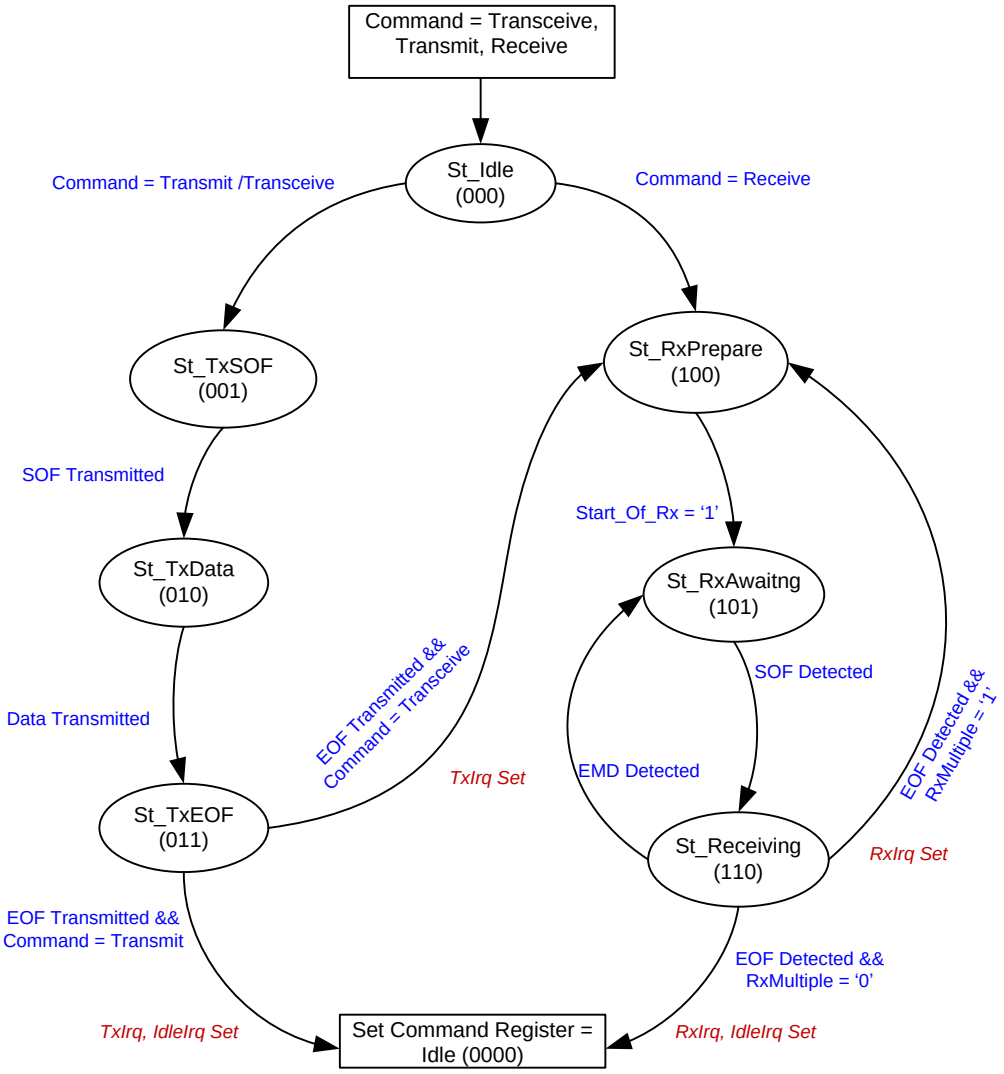


Figure 7-6: State diagram in ***Transceive***, ***Transmit*** and ***Receive*** command

7.6 WriteEEPROM Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x01	Write data in the FIFO buffer to the EEPROM	Start Address + Data stream	-	TxIrq, IdleIrq

The ***WriteEEPROM*** command gets data from the FIFO and programs into the defined address in the EEPROM. The first argument in the FIFO is starting address to be programmed; the later bytes are data stream. After programming is complete, the **TxIrq** and **IdleIrq** are set. Note that this command cannot be terminated by the ***Idle*** Command. Like ***Transmit*** command, the FIFO-filling routine in the microcontroller must manage data segmentation, if the number of data to be programmed is more than 64 bytes at the same time. It is important to note that if the internal state machine found that the FIFO is already empty, the following written data stream is not programmed and remained in the FIFO buffer. If the input argument is incorrect, such as programming the write-only area or the number of argument less than two, the bit **AccessError** in the **Errorflag** register will be set. If programming fails by any reason, the bit **E2Error** in the **Errorflag** register is set to indicate a failure of programming. Programming is block-wise where each block of EEPROM contains 4 bytes. The programming time is directly proportional to the number of blocks that cover the starting and ending addresses. The programming time of one block takes 4.9 ms. Table 7-8 shows examples of programming arguments and their results.

Table 7-8: Examples of EEPROM arguments and results

Data in FIFO	Written Address	Written Data	Irq Flag	Error flag
0x06 + 0x5D	0x06	-	**IdleIrq**	**AccessErr** is set because of writing into Read-Only region.
0x10 + 0x03 + 0x15	0x10	0x03	**TxIrq, IdleIrq**	No Error flag is set.
	0x11	0x15		
0xFE + 0x52 + 0x97 + 0x21	0xFE	0x52	**TxIrq, IdleIrq**	**AccessErr** is set because of writing into Read-Only region (Address 0x00) in the last byte.
	0xFF	0x97		
	0x00	-		

7.7 ReadEEPROM Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x03	Read data from EEPROM and return in FIFO buffer	Start Address + the number of byte to be read	Data stream	IdleIrq

The ***ReadEEPROM*** command reads data from the EEPROM and returns read data to the FIFO. The first data in the FIFO defines the first address to be read. The next data states the number of bytes to be read. After the command starts, the memory data is returned to FIFO byte-by-byte until the reading reaches the defined number of bytes. Then, the state control switches to idle state and **IdleIrq** flag is set. Excluding overhead, the duration of one byte reading is 16 clock cycles. When the number of reading bytes is more than 64, the microcontroller must control the accessing routine to avoid FIFO overflow. If the input argument is incorrect, such as reading Write-Only address or the number of addresses is zero, the bit **AccessError** in **Errorflag** register is set. Table 7-9 shows examples of reading arguments and their corresponding results.

Table 7-9: Example case of ReadEEPROM and their results

Input Data FIFO	Returned data in FIFO	Result / Error
0x00 + 0x50	Data from byte address 0x00 to 0x4F	No Error flag is set.
0x10 + 0x00	-	Access Err is set because the number of address is zero.
0x60 + 0x52	-	Access Err is set because some addresses to be read are in write-only region. So, there is no execution from this command.

7.8 *CalcCRC* Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x12	Turn on CRC calculation process and data in FIFO buffer is calculated CRC	Data stream	-	IdleIrq

The ***CalcCRC*** command activates the CRC calculation of the data stream in the FIFO. The preset value is defined in registers **CRCPresetMSB** and **CRCPresetLSB,** and the calculation algorithm is configured by the **ChannelRedundancy** register. After the calculation is completed, the calculation result is shown in registers **CRCResultMSB** and **CRCResultLSB** and the flag **IdleIrq** is set. This command is automatically terminated when the FIFO is empty. If the data stream is more than 64 bytes, the microcontroller should continuously feed the data to the FIFO as in ***Transcieve*** command.

7.8.1 CRC 16-bit

When bit **CRC8** (0x22.4) is set to 0, CRC coprocessor performs 16-bit CRC calculation. The polynomial for 16-bit CRC calculation is $X^{16}+X^{12}+X^{5}+1$. For ISO14443A, bit CRC3309 (0x22.5) must be set to 0. For ISO14443B and ISO15693, bit **CRC3309** (0x22.5) must be set to 1. If bit **CRC3309** is set, final CRC value is xored with 0xFFFF based on ISO/IEC3309.

7.8.2 CRC 8-bit

When bit **CRC8** (0x22.4) is set to 1, CRC coprocessor performs 8-bit CRC calculation. The polynomial for 16-bit CRC calculation is $X^{8}+X^{4}+X^{3}+X^{2}+1$**.** Preset value for 8-bit CRC calculation is defined in **CRCPresetMSB** (0x23)**.** The output from CRC calculation is displayed in **CRCResultMSB**.

7.9 LoadConfigEEPROM Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x07	Read data from EEPROM and initialize to register page	Starting Address	-	TxIrq, IdleIrq

The ***LoadConfigEEPROM*** command reads 32 byte address starting from the address defined in the FIFO and copied into the register page from the register 0x10 to 0x2F. After all data is copied into the register page, the flag **IdleIrq** is set. If the input argument is incorrect, i.e., the EEPROM addresses to be loaded are in write-only (read-protected) region, the bit **AccessError** in **Errorflag** register is set. Table 7-10 shows examples of ***LoadConfigEEPROM*** with various starting addresses and their results.

Table 7-10: Example cases of Result after executing ***LoadConfigEEPROM***

Data in FIFO	Address of reloaded memory	Error
0x0A	0x0A to 0x39	-
0x10	0x10 to 0x2F	-
0x24	0x24 to 0x43	-
0x50	-	Access Err, some address bytes in write-only (read-protected) region

7.10 LoadKeyFIFO Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x19	Read data in FIFO and put into a key buffer	Byte0 (LSB) + Byte1+… +Byte10+Byte11	-	TxIrq, IdleIrq

The ***LoadKeyFIFO*** command reads 12-bytes data in the FIFO. The data must be in key storage format. If the data format is correct, then the key is loaded into the internal key buffer and the bit **KeyError** in the **Errorflag** register is cleared, otherwise it will be set. When this command is finished, bits **TxIrq** and **IdleIrq** are set. The FIFO cannot be accessed from the external microcontroller while this command is executed.

7.10.1 Key Format

Before execution of the ***LoadKeyFIFO*** or ***LoadKeyEEPROM*** command, a specific key format must be written into the FIFO or stored in the EEPROM, respectively. Each byte of the 6-byte Crypto_M key must be split into 4 MSB, high nibble, and 4 LSB, low nibble. Each nibble is written in one byte, containing its inverted bit version in high nibble and itself in low nibble. An example of the key format is shown in Table 7-11.

Table 7-11: Example of the key format

Key (Hex)	Data Written to the FIFO (Hex)
F0 F1 F2 F3 F4 F5	**0F F0 0F E1 0F D2 0F C3 0F B4 0F A5**
A2 B8 73 93 64 CF	**5A D2 4B 78 87 C3 69 C3 96 B4 3C 0F**

7.11 LoadKeyEEPROM Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x0B	Read data from EEPROM and put into a key buffer	Start Address	-	TxIrq, IdleIrq

The ***LoadKeyEEPROM*** command reads 12-byte data from the EEPROM started from the defined address byte in the FIFO and put into the key buffer. The reloaded data must be in the key storage format as shown in Table 7-11. If the key format is incorrect, the bit **KeyError** in the **Errorflag** register is set. When all keys are loaded into a key buffer, this command is automatically terminated and the flags **TxIrq** and **IdleIrq** are set.

7.12 *Authent* Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x0C	Execute the authentication between reader and card	Card's Authent command + Card's Block address + Card's UID(LSB) + … + Card's UID(MSB)	-	IdleIrq TxIrq RxIrq

The ***Authent*** command executes the authentication routine to card(s) containing Crypto_M engine. It is a combination of 2 consecutive transactions between reader and card. This command requires six byte data in arguments consisting of card authentication command, the address of blocks to be authenticated, and the card UID repectively. Before executing this command, the associated key must be loaded in to the key buffer. In the first part of the authentication process, six byte data in the FIFO is transmitted to the card. The card response is verified. Then, the second transaction is performed. The verification output from the first response is retransmitted to the card. The second card response is verified again. If all verifications are complete, the bit **Crypto_MOn** in the **Control** register is set to indicate the completion of the authentication, and all communications onwards will be encrypted. This bit cannot be set directly by the external microcontroller, except the execution from the Authent command. Moreover, interrupt flag IdleIrq, TxIrq and RxIrq are set in case of authentication successful after Authent command is finished. If the authentication is unsuccessful, some interrupt flags are set depending on RF event as shown in Table 7-12.

Table 7-12: Interrupt flag result from ***Authent***-command

RF Event	Interrupt Flag	Crypto_MOn
No card response*	TimerIrq	0
No Card response in second transaction*	TimerIrq, TxIrq	0
Wrong response in Second transaction	TxIrq, IdleIrq, RxIrq	0
Complete authentication	TxIrq, IdleIrq, RxIrq	1

* In this case, the value in command register is still in ***Authent***-command state.

7.13 *TuneFilter* Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x10	Activate the filter-frequency-corner-tuning process in receiver amplifier	-	-	**IdleIrq**

The ***TuneFilter*** command activates the filter-frequency-corner-tuning process in the receiver amplifier. This command is for adjusting the filter frequency corner due to variations in temperature and manufacturing process. After operating the command, all frequency corners are set back to the proper values and the frequency deviation is eliminated. The tuning process takes 302uS. However, this command is automatically performed every time the system is powered up. Hence, it is not required to tune the filter by users frequently.

8. Typical operating circuit and Design consideration

8.1 Circuit configuration

Typical circuit configuration of the RE31 for closed coupling is shown in Figure 8-1. The transmitter is set to drive a differential antenna from pin **TX**1 and **TX2** , and the internal envelope detector is employed. L1, C1, C2 and C3 form a transmitter antenna matching network, while LAnt is a loop antenna, which can be realized by a PCB trace. The signal tapping point for the receiver is directly from the loop antenna via C4. R1 and R2 are used as a carrier-divider to feed the receiver input signal to the pin **RX**. Signal swing must be divided properly and accommodated within an operating range of the internal envelope detector. C5 is a decoupling capacitor for mid rail reference voltage. Defined from the baseband line coding, the bandwidth of the antenna network should be wide enough to cover the bandwidth of both transmission and reception to prevent inter-symbol interfere. For examples, ISO14443A and ISO14443B require the bandwidth around 1 MHz, while ISO15693 requires only 500 kHz. Reciprocally, rising and falling time of the modulation in the transmission must be within a limit of an operating standard. Note that the input pin **SIGIN[0]** and **SIGIN[1]** must be tied to ground in the normal operation. Examples of component values to cover the bandwidth of all standards are shown in Table 8-1 as a guideline. However, the antenna network fine trimming is required to meet specifications for each an operating standard especially for rising time, falling time, and overshoot of transient response of carrier.

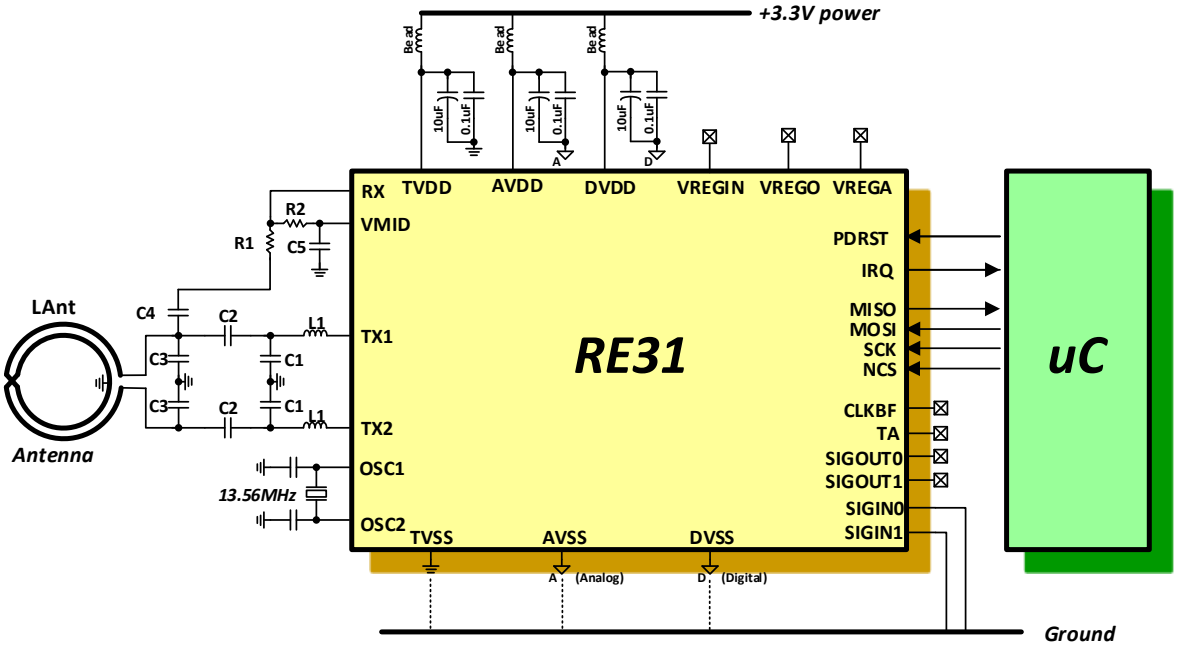


Figure 8-1: Typical circuit configuration of RE31 for closed coupling

Table 8-1: Example of component values to cover bandwidth

Component	Example 1	Example 2
LAnt	0.4 uH (Q=50)	0.4 uH (Q=50)
L1	0.47 uH	0.33 uH
C1	260 uH	370 pF
C2	33 pF	47 pF
C3	650 pF	645 pF
C4	1nF	1 nF
C5	100 nF	100 nF
R1	1 kohm	1 kohm
R2	180 ohm	180 ohm

Moreover, the RE31 is capable of connecting to various RF topologies. The transmitter driver can be designed to connect to not only a differential-drive antenna but also a single-ended-drive antenna, and a class-E amplifier. Figure 8-2 illustrates possible driver connections. The differential and single-ended types are suitable for driving an on-board antenna for closed coupling applications. The single-ended with 50-ohm output matching and a class-E amplifier are used for connection to a remote antenna through 50-ohm cable. In addition, the class-E amplifier can provide high power required by mid/long range reader. The RE31 transmitter supports in-phase driving for a single-ended or plain carrier and a base band in class-E topology.

The RE31 is capable to receive demodulated baseband from an external envelope detector. Employing the external envelope detector can yield better sensitivity than performing through the internal one because large amount of carrier is removed, while the baseband signal is not significantly attenuated comparing to the carrier dividing scheme. Note that the register **BypassENV** must be set if the external envelope is used. A simple external envelope detector connection is shown in Figure 8-3. For an on-board antenna reader, the signal tapping point for the receiver is typically at the antenna where the largest modulation from card presents. For 50-ohm cable driving type in which the antenna is located remotely, the tapping point can be selected from one of the local points (i.e., A, B, or C) where the largest modulation exhibits.

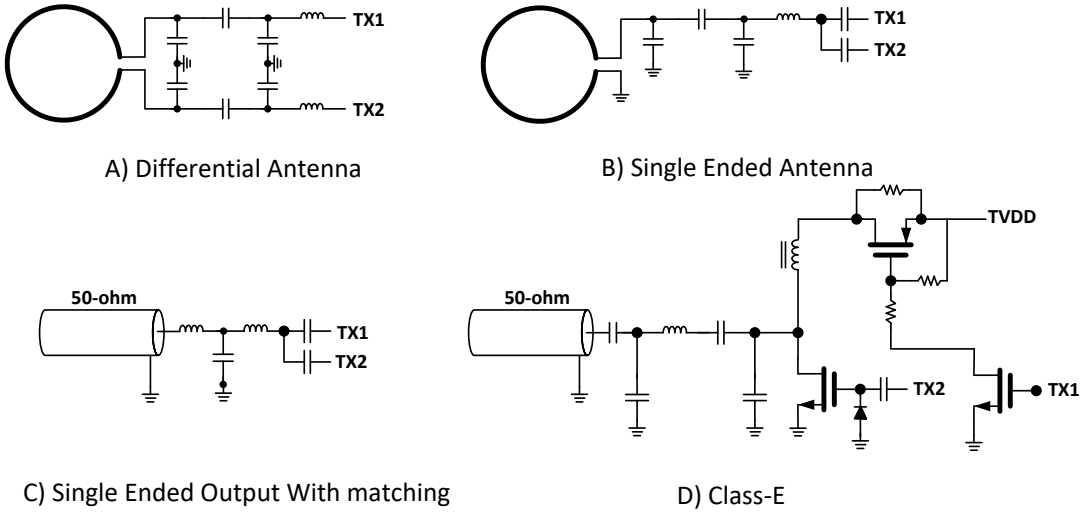


Figure 8-2: Various transmitter configurations that RE31 supports

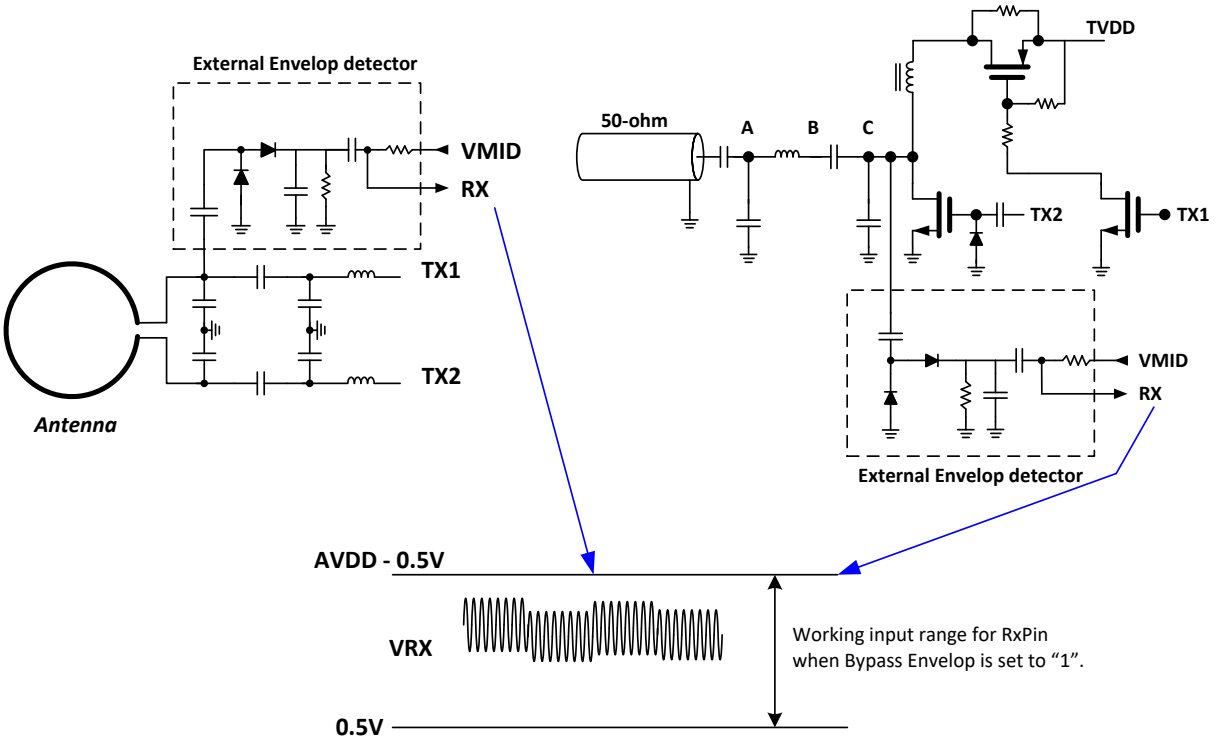


Figure 8-3: External envelope detector connection

8.2 Power supply & Grounding

In RFID systems, the receiver extracts the card-response signal from the envelope of the RF carrier on the antenna. Except for some smartcards where their operating range is deliberately limited by their designs, the noise in transmitter, which inevitably reflects back to receiver system, is a limiting factor for the reading performance, especially in ISO15693. The noise in the transmitter is mainly stemmed from the transmitter power supply ripple and clock jitter. The clock jitter is from the analog power supply noise, in which the oscillator relies on, and the cleanliness of the clock source.

To achieve the highest reading performance, the noise in both transmitter and receiver section should be as low as possible. The noise in the receiver is fundamentally limited to electronic noise as stated in Table 3-6. Hence, common techniques, such as power supply separation, decoupling capacitor and grounding, should be employed. The RE31 provides three power-supply sets for a transmitter, an analog part, and a digital part. Positive power supply of each part can be simply separated by ferrite beats. A more effective measure is to use dedicated regulators to block the noise feeding through other parts. Local decoupling capacitors, 10-uF tantalum and 0.1-uF ceramic, must be provided to supply high-frequency current and placed close to each power supply input. In floor-planning, external high-current sections, unrelated to RF transmission and noise-generating components, must be grouped and placed far away from sensitive analog parts such as oscillator, external envelope detector, and RF transmitter. For example, the high current component can be a switching power supply, while the noise generating component can be a microcontroller or host interface components. For RFID reader applications, the analog ground AVSS and the transmitter ground TVSS must be on the same ground to keep the same potential for both the receiver and the transmitter. Physically, the analog and transmitter ground can be connected by a unified solid ground plane. As typical technique used in mixed-signal system, the analog part and the digital part, digital section of the RE31 and the external microcontroller, can be on the same ground plane. However, the power source direction and the ground return path from such noisy components should be carefully designed to avoid current superimposition causing a bouncing between the analog and the transmitter ground. A switching power supply and a heavy driver for the interface must be placed on the isolated ground plane with the isolated return path. In case of the switching power supply, the operating frequency must carefully be designed so that it is not overlap the operating bandwidth. Magnetic shield inductor and component selection can be employed to reduce such effect.

8.3 Test Signal

For Manchester-and-FSK decoder in ISO14443A and ISO15693, the purpose of test signal is for monitoring and fine-tuning the time wait, Twait, between EOF of the transmitted data and SOF of the received data. The Twait, defined by registers **Bitphase** and **Rxwait,** must be synchronously set to make the decoder evaluate correctly. For BPSK decoder, the Twait must be set to assert before SOF of the card response. Also, some test signals can be used to see phase distortion from the antenna and its effect. Table 8-2 summarizes key test codes for configuring the register **Test[5:0]** (0x0A.[5:0]) to route internal key signals to monitor for adjustment of the above parameters. The meanings of such signals are explained in Table 8-3.

Table 8-2: Key test signal and indication

TestCode[5:0] (Hex)	Pins				
	TA		SIGOUT[0]	SIGOUT[1]	Signal From Block
	Signal Name	From Block	Signal Name	Signal Name	
0x10	***OUT3P***	Amplifer	***RESET_INT***	***Start_Of_Rx***	Man/FSK decoder
0x11	***OUT3P***	Amplifer	***BPSK_SYN***	***BPSK_CLK***	BPSK Decoder
0x12	***OUT3P***	Amplifer	***VALID_OUT***	***CLK_OUT***	Man/FSK/BPSK Decoder
0x13	***OUT3P***	Amplifer	***DATA_OUT***	***CLK_OUT***	Man/FSK/BPSK Decoder
0x1E	***VRECT***	Man/FSK decoder	***CORR_VALID***	***CORR_CLK***	Man/FSK decoder
0x1F	***VERCT***	Man/FSK decoder	***CORR_COLL***	***CORR_CLK***	Man/FSK decoder

Figure 8-4 shows three internal signals during Manchester-coding reception in ISO14443A, namely ***Start_Of_Rx*** used in starting Manchester-and-FSK decoding, ***RESET_INT*** used in resetting evaluation results of each half bit and input analog signal, and ***OUT3P*** for the Manchester-and-FSK decoder. Also, the ***OUT3P*** is the amplifed envelope from the last amplifier state. Active state of ***RESET_INT***, indicating point in resetting for each half bit, must be set to coincide with the beginning point the Manchester-and-FSK-decoder input signal burst, ***OUT3P***. By adjusting registers **Bitphase** and **Rxwait**, the proper alignment of ***OUT3P*** and ***RESET_INT*** as shown in Figure 8-4 can be achieved. This results in a complete integration of each half bit as shown in Figure 8-5 and yields better discrimination in case of anti-collision. Note that the period of ***RESET_INT*** is equal to half ETU of the operating standard. Figure 8-5 shows the valid evaluation result ***VALID_OUT*** while Figure 8-6 displays the collision result ***CORR_COLL***.

Table 8-3: Meaning of Key test signal

OUT3P	An amplified output from the 3rd state amplifier
VRECT	An integrated output from Manchester decoder. The last value of ***VRECT*** is used to evaluate the output bits together with **Minlevel** and **Collevel.**
RESET_INT	Signal indicating new slots used in Manchester decoder
Start_Of_Rx	Signal for Manchester decoder to start evaluating incoming bits
BPSK_SYN	Recovery BPSK signal from DPLL
BPSK_CLK	Recovery Clock of input BPSK signal from DPLL
VALID_OUT	Validity of output data
DATA_OUT	Evaluate output data
CLK_OUT	Signal showing clock of output data
CORR_VALID	Validity of output data from Manchester decoder
CORR_COLL	Collision of output data from Manchester decoder
CORR_CLK	Clock for output data from Manchester decoder

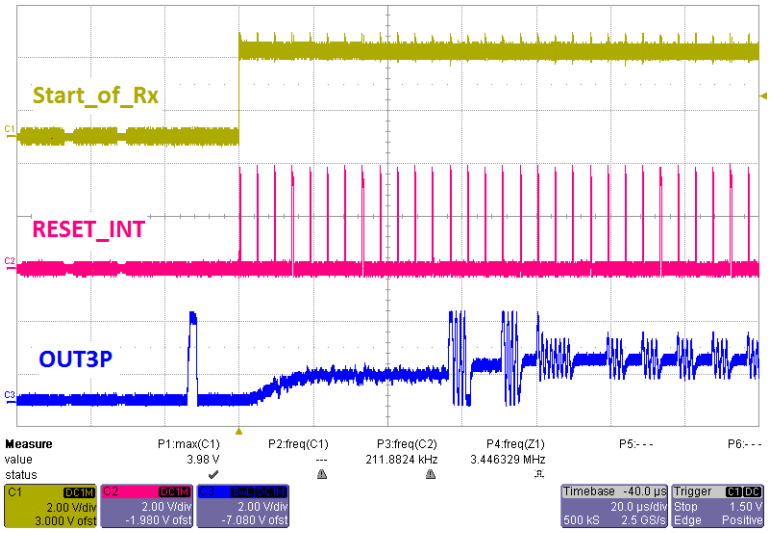


Figure 8-4: ***OUT3P***, ***Reset_Int*** *and* ***Start_Of_Rx*** (**Test** register is set to 0x10)

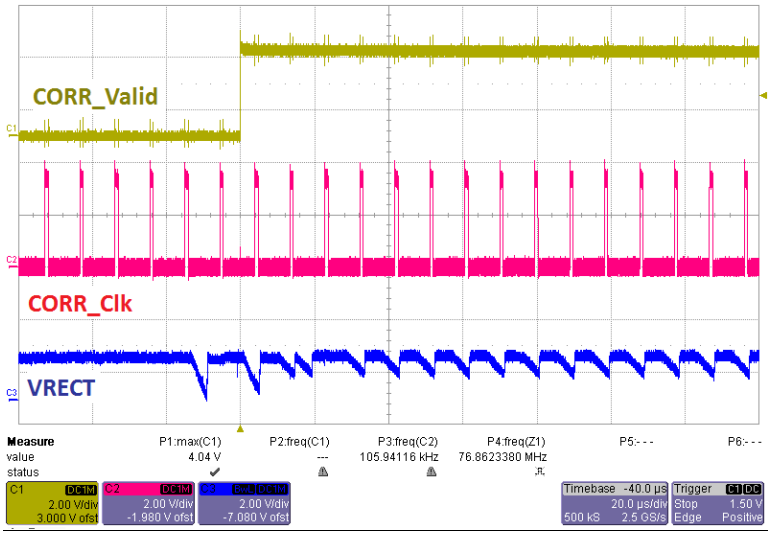


Figure 8-5: ***VRECT***, ***CORR_Valid*** *and* ***CORR_Clk*** (**Test** register is set to 0x1E)

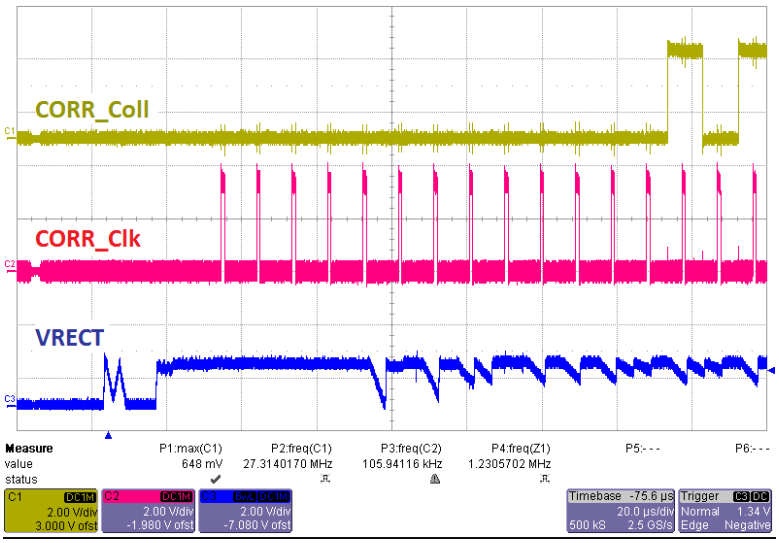


Figure 8-6: ***VRECT***, ***CORR_Coll*** *and* ***CORR_Clk*** (**Test** register is set to 0x1F)

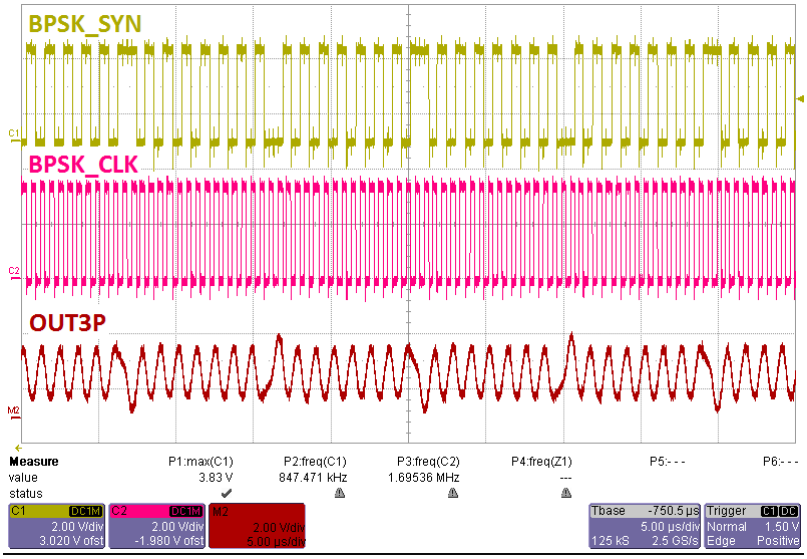


Figure 8-7: ***OUT3P***, ***BPSK_Syn*** *and* ***BPSK_Clk*** (**Test** register is set to 0x11)

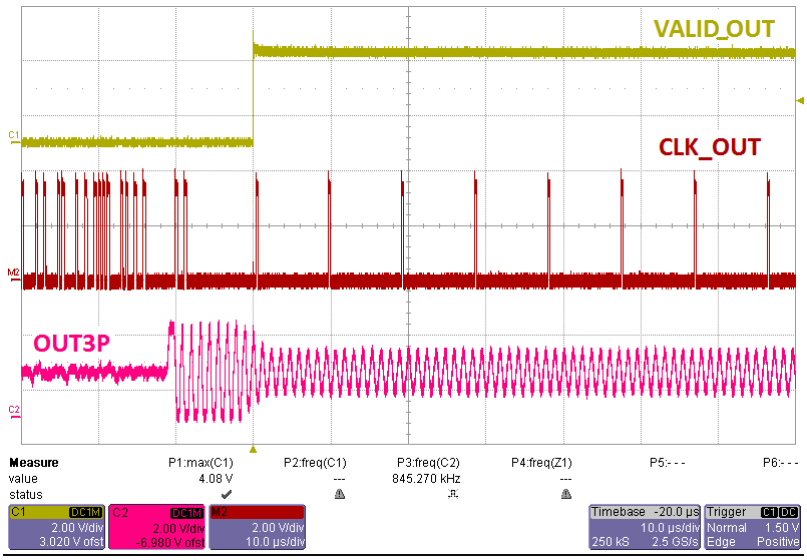


Figure 8-8: ***OUT3P***, ***Valid_Out*** *and* ***Clk_Out*** (**Test** register is set to 0x12)

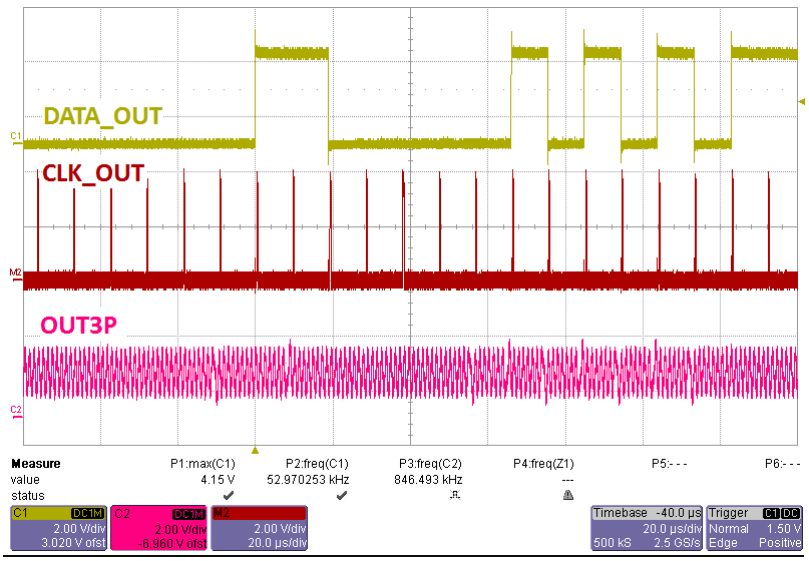


Figure 8-9: ***OUT3P***, ***Data_Out*** *and* ***Clk_Out*** (**Test** register is set to 0x13)

For BPSK coding in ISO14443A at higher rate and ISO14443B, users can monitor evaluation results from BPSK decoder as shown in Figure 8-7, Figure 8-8 and Figure 8-9. Figure 8-7 shows the amplified envelope signal ***OUT3P*** and synchronous BPSK data from the slicer ***BPSK_SYN*** as well as the recovery clock ***BPSK_CLK***. Figure 8-8 and Figure 8-9 show valid evaluation results ***VALID_OUT*** and evaluated data ***DATA_OUT*** as well as its recovery clock and the amplified envelope ***OUT3P***. Apart from timing setting as in Manchester, another purpose in monitoring BPSK signal is for adjusting the system if the evaluation result disagrees with the expected value due to phase distortion. The ***OUT3P*** can exhibits the effect of phase distortion in subcarrier from the antenna transfer function, the internal filter, and the amplifier while ***BPSK_SYN*** and ***BPSK_CLK*** show evaluation results if such distortion can be tolerated. Examples of adjustments may be required such as the bandwidth of the antenna matching network, the time constant of DPLL or even the frequency corner filter. However, in normal situation, such adjustment is hardly necessary.

8.4 Thermal consideration

Silicon temperature during operation should not exceed the maximum limit at 125 C for best performance and long term reliability. The operating temperature of the silicon (T_J) can be calculated from total power consumption (P_{lossT}), thermal impedance (θ_{JA}) and ambient temperature (T_A) according to the following equation below.

$$T_J - T_A = \theta_{JA}. P_{lossT}$$

Depending on power loss, the heat sink structure and heat dissipation path must be sufficiently provided to maintain the silicon temperature within the maximum operating range.

The transmitter and regulator are the main heat source of the RE31. Then, the total power consumption is approximately the sum of power loss from both parts.

$$P_{lossT} = P_{lossTX} + P_{Reg}$$

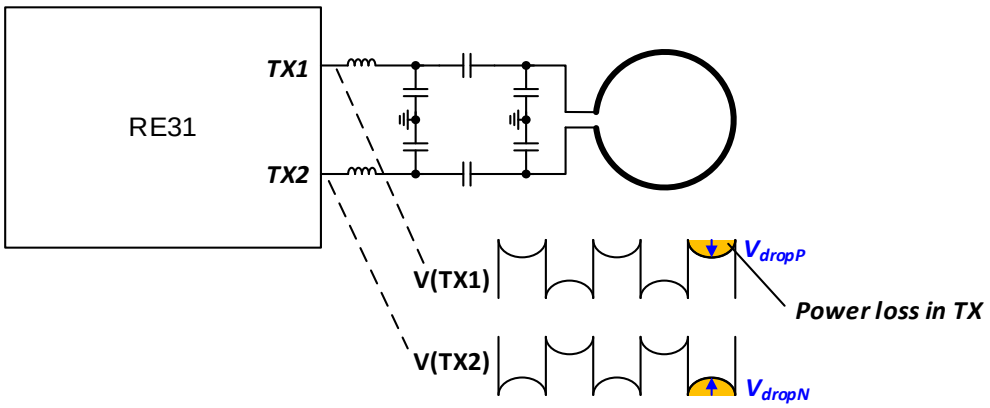
For the first part P_{lossTX}, assuming worst case scenario, the transmitter drives the effective resistive load at the operating frequency. Thus, the sourcing and sinking current can be approximated to be half-sinusoidal shape as illustrated in Figure 8-10. Hence, the power loss from voltage drop across the driver is

$$P_{lossTX} = (I_{out})^2. R_{out}$$

Where

I_{out} is a peak output current from the driver,

R_{out} is an effective resistance of the driver output.



Assume load is resistive at carrier frequency

$$P_{lossTX} = (½)\frac{V_{dropP}^2}{R_{outP}} + (½)\frac{V_{dropN}^2}{R_{outN}} = \frac{V_{drop}^2}{R_{out}} = I_{out}^2 R_{out}$$

By approximation: $V_{dropP} \cong V_{dropN}$, $R_{outP} \cong R_{outN}$

Figure 8-10: Power loss from the transmitter

Similarly, the above loss calculation can also be used in the single-ended configuration. For other configurations, the power loss in the transmitter must be calculated case-by-case depending on structure of the external circuit. For example, if an external amplifier is a class-E as shown in Figure 8-10, the power loss in the RE31 transmitter can be calculated from the switching loss, i.e.,

$$P_{lossTX} = V_{TX}^2 .f . C_{in}$$

Where

V_{TX} is an operating transmitter supply voltage,

f is an operating frequency which is 13.56 MHz,

C_{in} is an input capacitance of MOSFET.

For the second part of the power loss P_{Reg} , the loss in the regulator can be calculated from the dropout voltage multiplying by the passing current.

$$P_{Reg} = I_{Out,Dig}.(V_{InReg} – V_{OutReg}) + I_{Out,Ana}.(V_{InReg} – V_{OutReg})$$

For example, the transmitter is designed to drive a differential antenna from a 5-Volt power supply and deliver 200 mA peak output current. Both regulators supply 80 mA output current by relying on 5V input.

From Table 3-5, the effective resistance of the driver output is approximately at 10 ohm, the transmitter loss is

$P_{lossTX} = (0.2)^2 \times 10 = 0.4$ watt.

For the regulator, the loss is

$P_{Reg} = 2 \times (80mA \times (5V - 3.3V)) = 0.272$ watt.

The temperature coefficient θ_{JA} of an operating PCB is 36C/W. (Table 3-1)

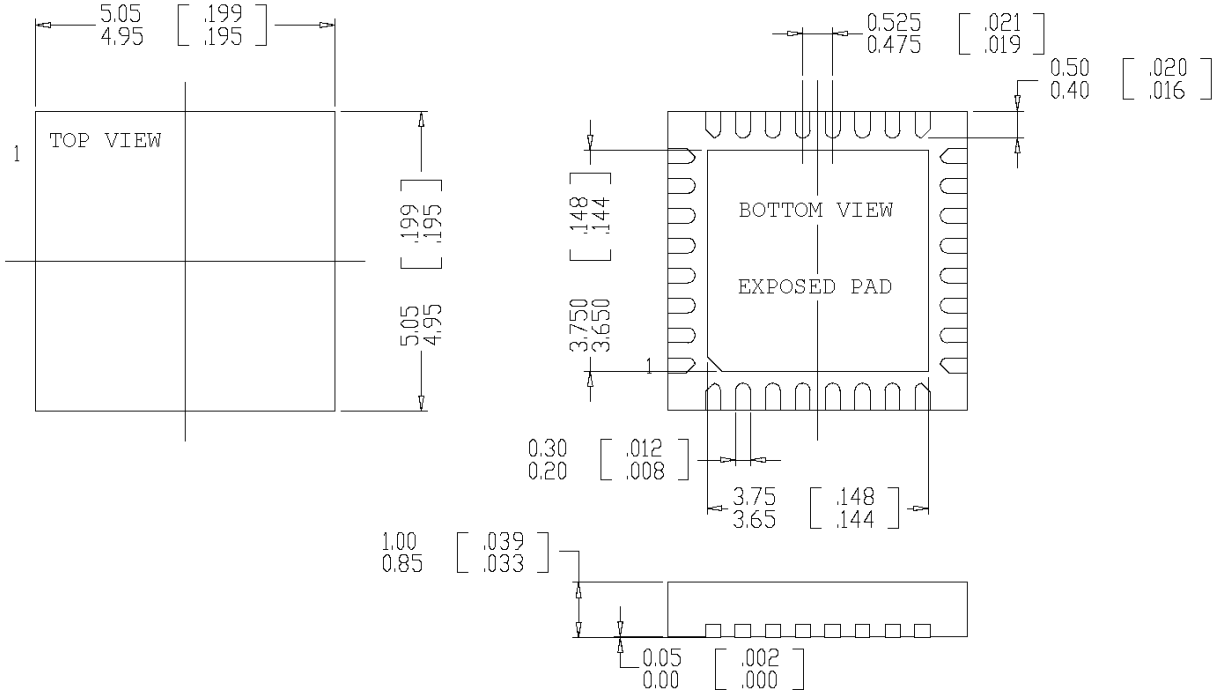
The different temperature between the silicon and ambient $T_J - T_A$ is

$T_J - T_A = (36C/W) *(0.4 + 0.272) W = 24.2$ C

T_J is set to 85 C. Then, the maximum T_A is approximately 60 C.

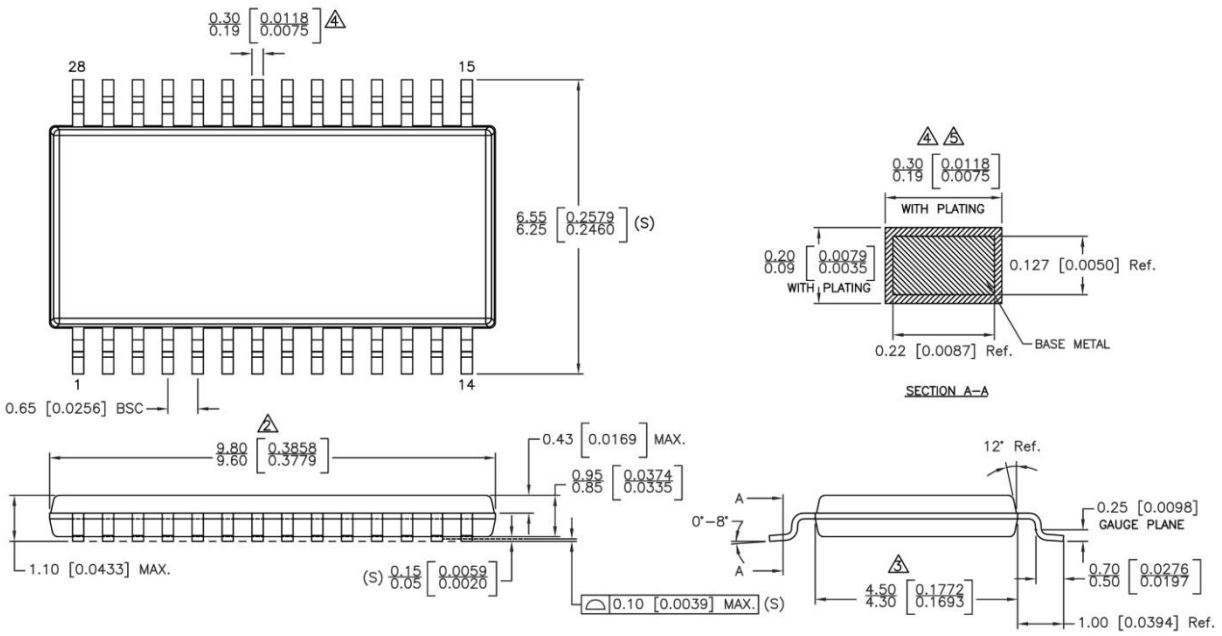
Practically, the designed PCB may be smaller from that stated in the JEDEC51-7 standard, so the temperature coefficient can be higher than the specification in Table 3-1 (36C/W). Designers must provide a proper heat sink with some margins to accommodate elevated temperature coefficient.

9. Packaging and Dimension



NOTE : CONTROL DIMENSION IN MM. DIMENSION IN BRACKET IS INCH.

Figure 9-1: Package dimension



NOTE:

1. CONTROLLING DIMENSION IN mm. [Inches.]

Figure 9-2: 28 Lead TSSOP Package dimension

10. Disclaimer

- The information described herein is subject to change without notice.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- Silicon Craft Technology assumes no responsibility for the way in which this IC is used in products created using this IC or for the specifications of that product, nor does Silicon Craft Tech. Assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Thailand or in other countries.
- Silicon Craft Technology is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Silicon Craft Technology is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Silicon Craft Technology.
- Although Silicon Craft Technology exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.